

Compal Confidential

Model Name : SAGE
Compal Project Name : V1JV1
File Name : LA-9011P

Compal Confidential

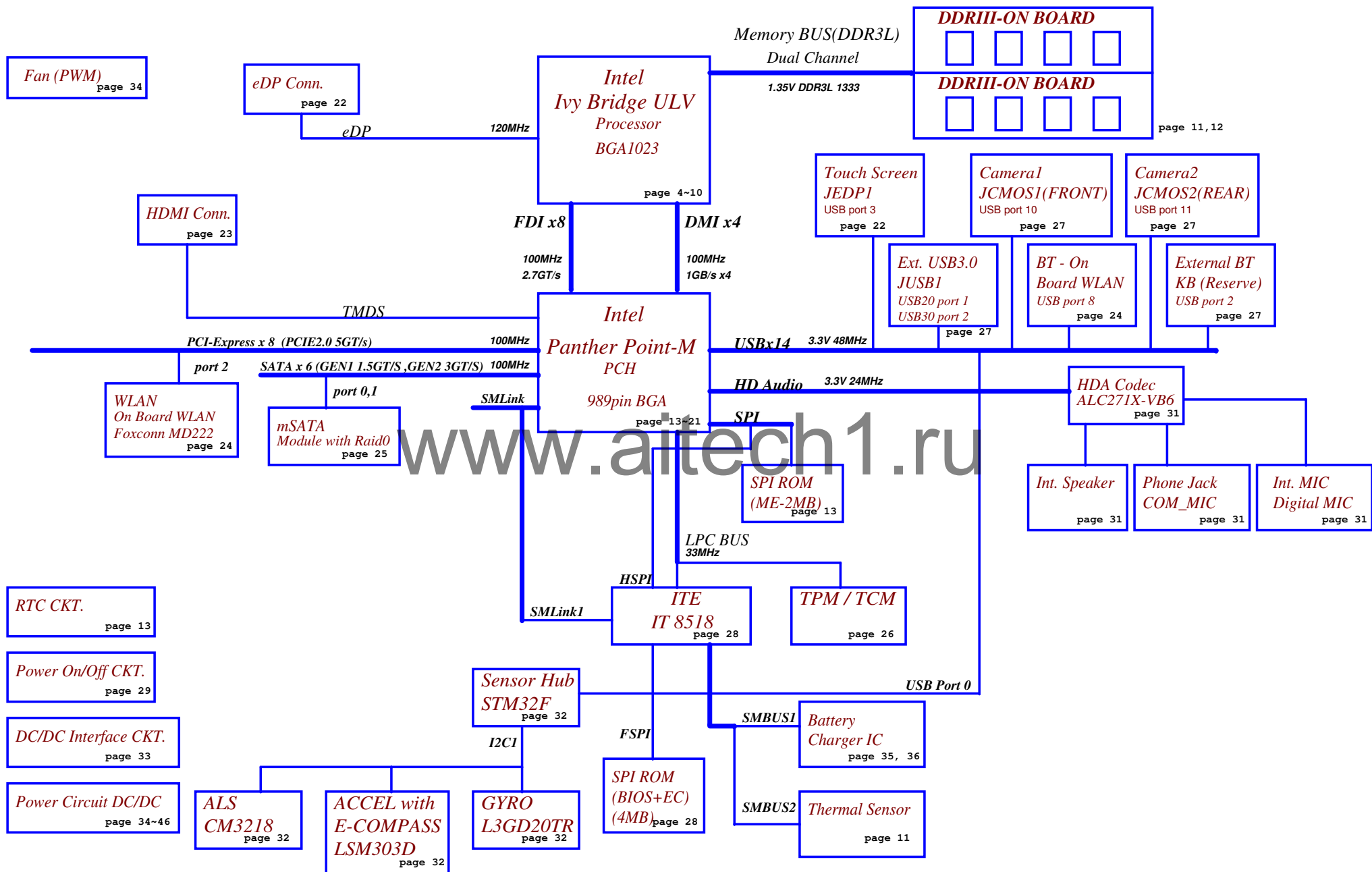
SAGE / V1JV1 UMA M/B Schematics Document

Intel Ivy/Sandy Bridge SFF BGA 1023p Processor
/Panther Point 989p PCH
/ DDR3L Memory Down *8

2012-08-20

REV : 1 . 0

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Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title Cover Page	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.35VS	+1.35V to +1.35VS switched power rail	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS power rail for PCH	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8VS switched power rail for PCH	ON	OFF	OFF
+3VALW	+3VALWP to +3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW always on power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VS	+VSBP to +VS always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
PCH SM Bus address	
Device	Address
ChannelA	A0 1010 000X
ChannelB	A4 1010 010X

EC SM Bus2 address

Device	Address
Gyroscope	D1 1101 000X b
D3	1101 001X b
E-compass + G sensor	33 0011 001X b
ALS sensor	21 0010 000X b

Sensor HUB SM Bus address

BOM Config

Sensors List

Connect to	Function	Device
Sensor Hub	Gyroscope	ST - L3GD20TR
Sensor Hub	Accel+E-Compass	ST - LSM303DLHCTR
PCH (USB P3)	Sensor Hub	ST - STM32F103RCY6TP
Sensor Hub	ALS	Capella - CM3218

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	LA-9012P_R01
5	1.0*
6	
7	

Note : LA-9011P -> Sensor Fusion with Intel F/W
LA-9012P -> Sensor Fusion with ST F/W

USB Port Table

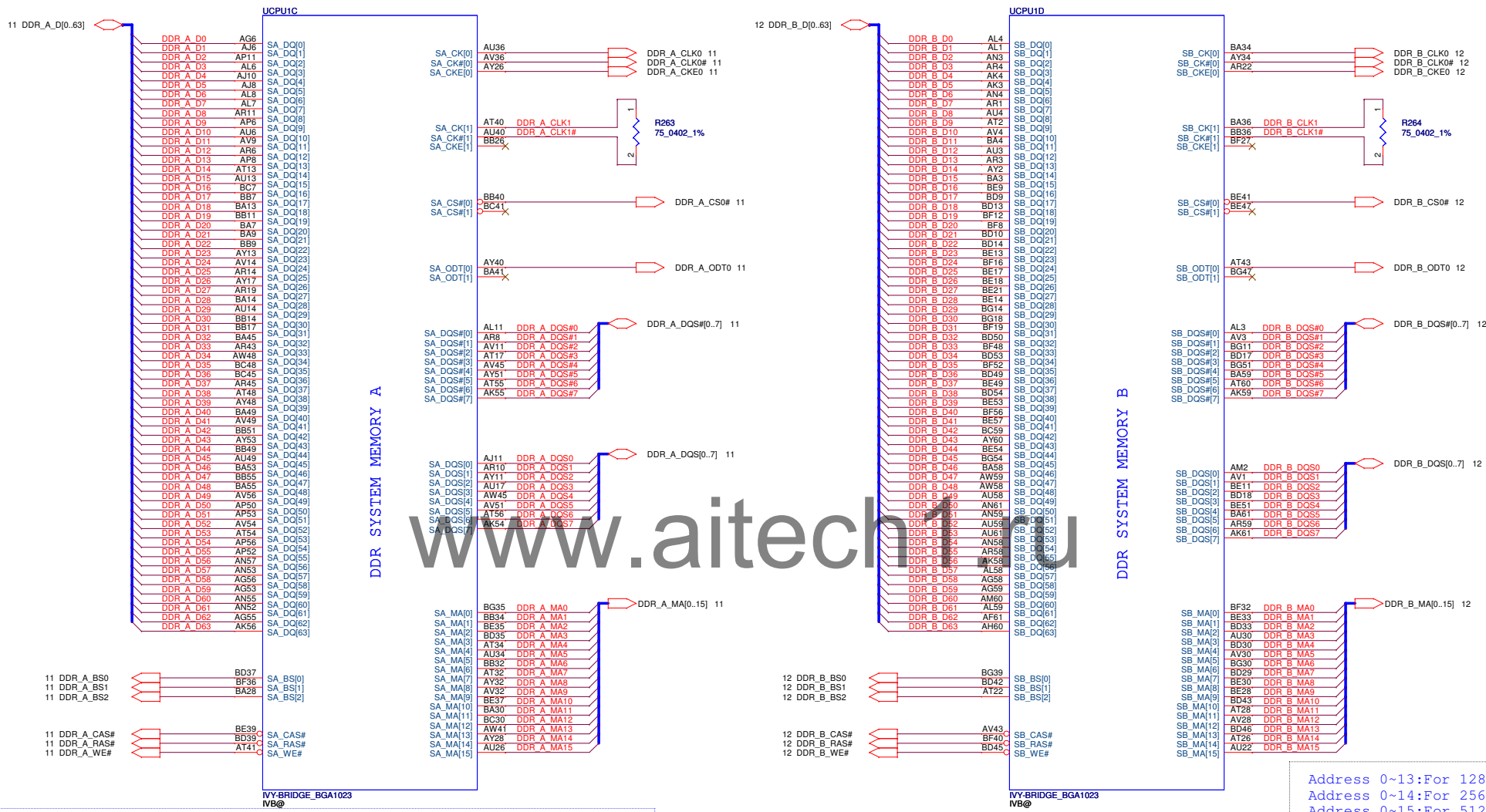
USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	Sensor Hub
		1	Ext. USB Connector
		2	Ext. BT KB (Reserve)
	UHCI1	3	Touch Screen
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	BlueTooth(WLAN Module)
	UHCI3	9	Debug Port(Reserve)
		10	Camera(Front)
		11	Camera(Rear)
	UHCI4	12	
		13	

BTO Option Table

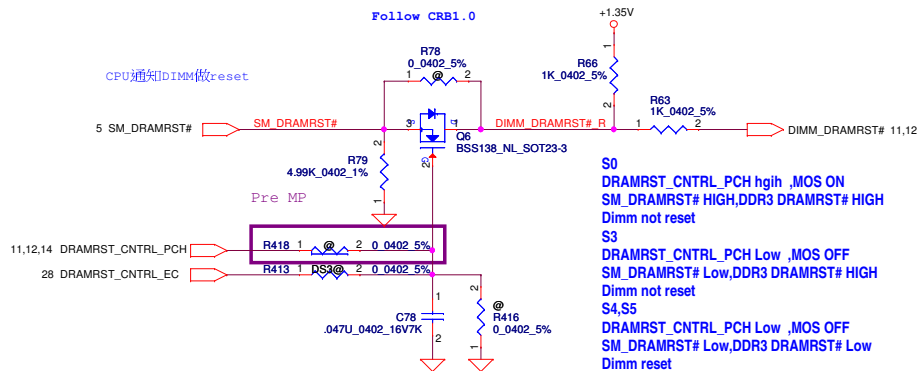
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA	UMA@
CPU	IVB@
DDR3	DDR3@
DDR3L	DDR3L@
On Board DRAM	X76@
M3 support	M3@
eDP	eDP@
LVDS	LVDS@
PCH	HM77@
USB2.0 Conn	USB2.0@
USB3.0 Conn	USB3.0@
Normal S3	S3@
Deep S3	DS3@
TPM+TCM	TXM@
TPM	TPM@
TCM	TCM@
Hall Sensor	LID@
Dual Channel DDR	128@
Foxconn MD222	FOXMD222@
Lite-On MD222	LIONMD222@

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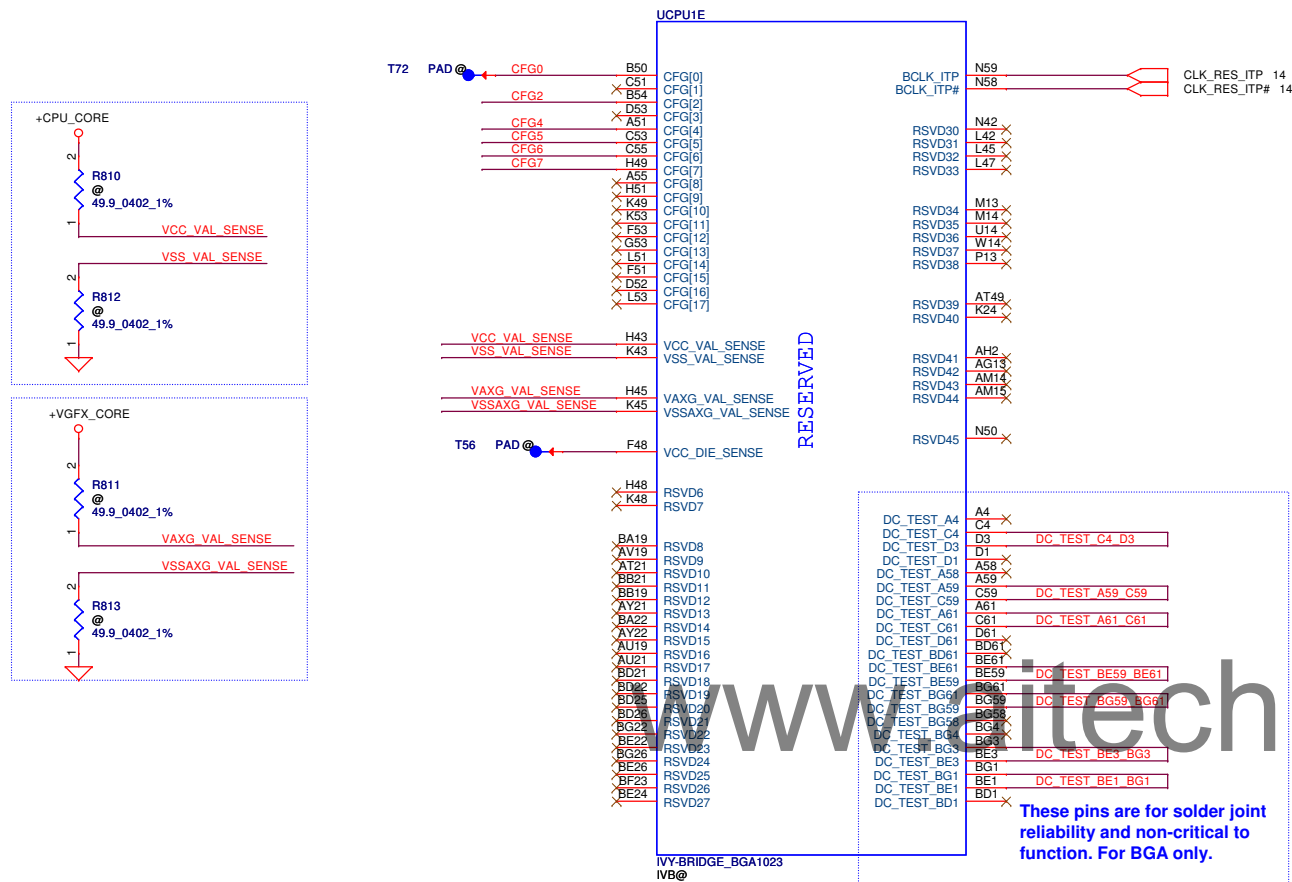
DIS only SKU or UMA eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT



Address 0~13:For 128*16
Address 0~14:For 256*16
Address 0~15:For 512*16



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Issued Date	2011/06/24	Deciphered Date	2012/06/02	PROCESSOR(3/7) DDRIII	
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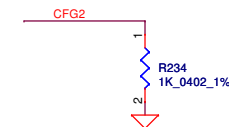


Default "1",EDS R1.0 P.88

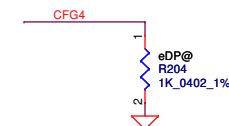
CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x

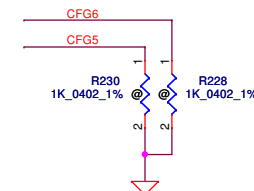
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed



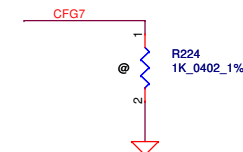
eDP enable	
CFG4	* 1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) 1x16 PCI Express
	10: 2x8 PCI Express
	01: Reserved
	00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	
CRB1.0 P.12	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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INTEL Recommend VCC
3*330uF,12*22uF(0805),16*2.2uF(0402)
PD0.9

ULV SC/DC 33A

UCPU1F

POWER

8.5A

INTEL Recommend VCCIO
PD 0.9

330uF 1+1
10uF (0603) *5
1uF (0201) *16

330uF 1
10uF (0603) *5
1uF (0201) *10

VCCIO_SEL For 2012 CPU support

A19 * 1 : +1.05VS_VTT
0 : +1.0VS_VTT

Check List R1.5
VIDALERT#:75ohm $\pm 5\%$ pull-up to VCCIO close to IMVP7
VIDSCLK: 55ohm $\pm 5\%$ pull-up to VCCIO close to IMVP7
VIDSOUT: 130ohm $\pm 5\%$ pull-up to VCCIO close to CPU
130ohm $\pm 5\%$ pull-up to VCCIO close to IMVP7

Check List R1.5
VCCSENSE:100ohm $\pm 1\%$ pull-up to VCC near processor.
VSSSENSE:100ohm $\pm 1\%$ pull-down to GND near processor.

Should change to connect from
power circuit & layout differential
with VCCIO_SENSE.

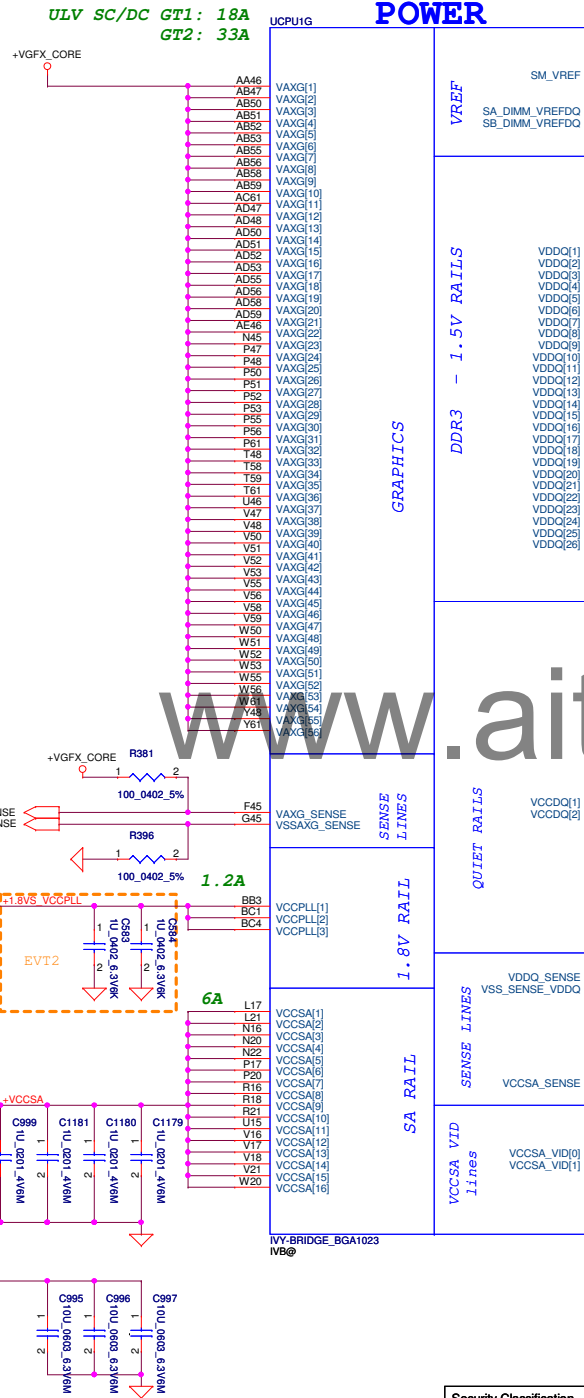
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Title					
PROCESSOR(5/7) PWR,BYPASS					
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Size		Document Number			
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INTEL Recommend VAXG
2*330uF,5*22uF(0805),6*10uF(0603),6*1uF(0402)
PD 0.9

Check List R1.5
VCCAXG_SENSE:100ohm \pm 5% pull-up to VCC near processor.
VSSAXG_SENSE:100ohm \pm 5% pull-down to GND near processor.

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD 0.9

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.9



SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandy bridge not support M3,
Check list1.0 & CRB say can NC

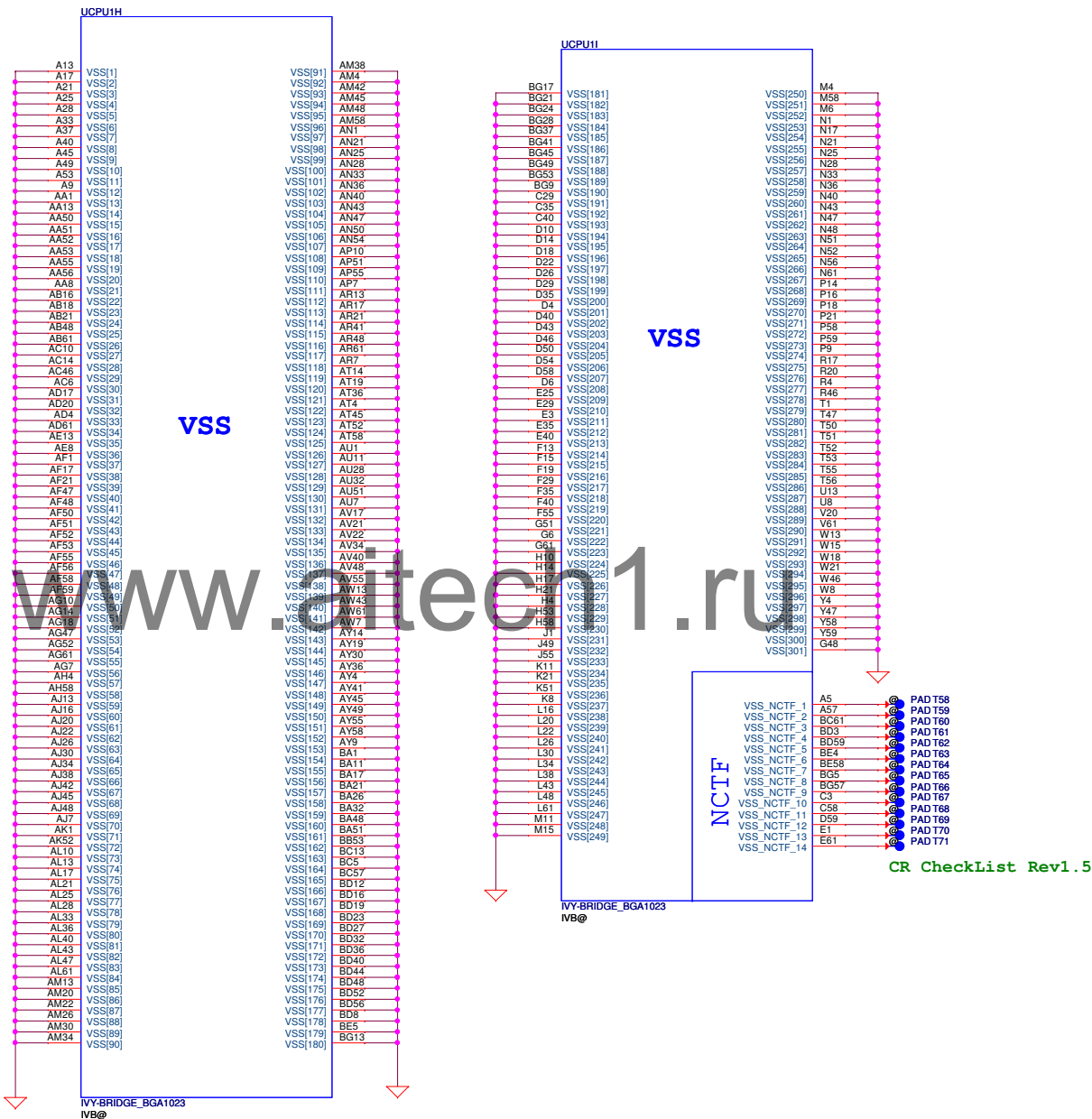
+V_SM_VREF should
have 20 mil trace width

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.9

Short for +1.35VS to +1.35V_CPU_VDDQ

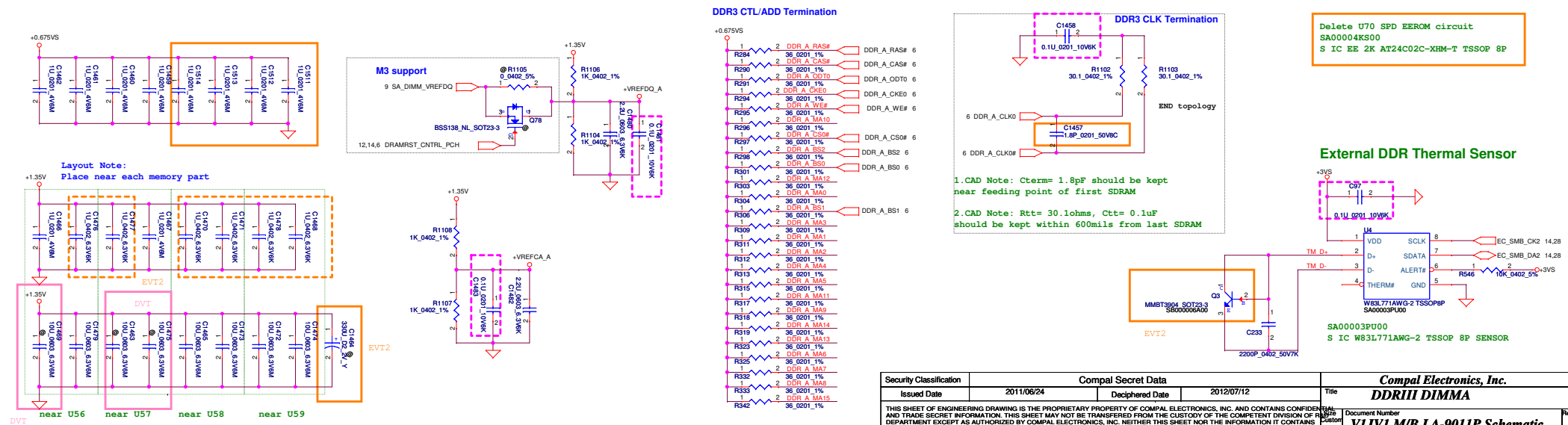
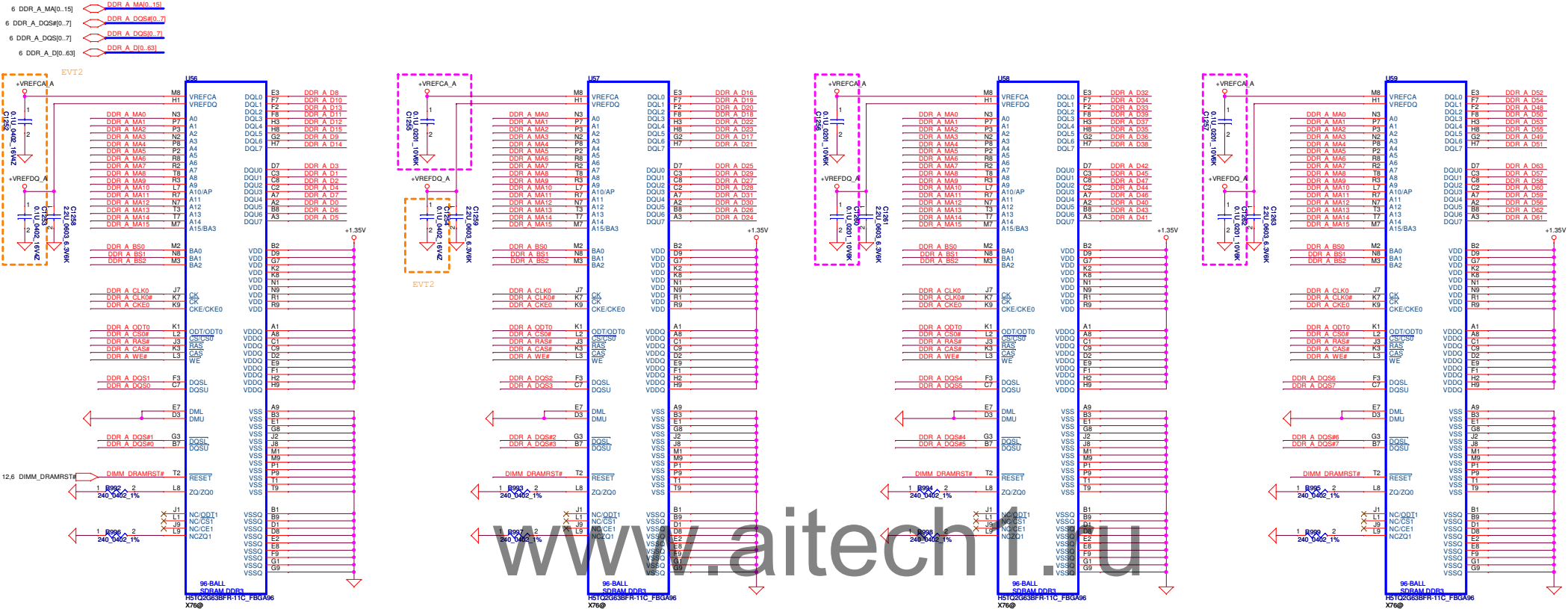
VCCSA_VID
For 2012 future CPU
VCCSA voltage select

VCCSA					
VID0	VID1	Vout	SNB	IVB	ULV
0	0	0.9V	V	V	V
0	1	0.8V	V	V	V
		0.85V			
1	0	0.725V	X	V	V
1	1	0.675V	X	V	V



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								PROCESSOR(7/7) VSS			
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Channel A

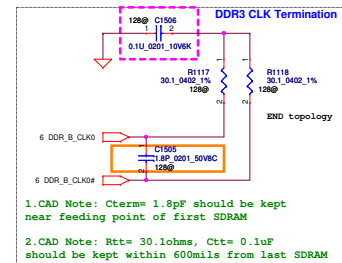


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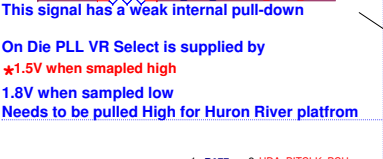
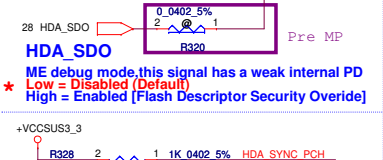
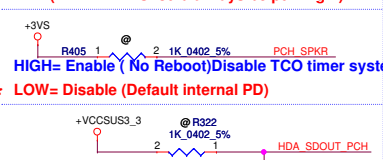
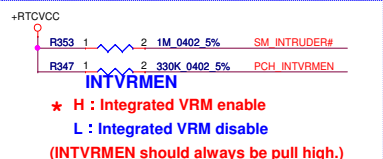
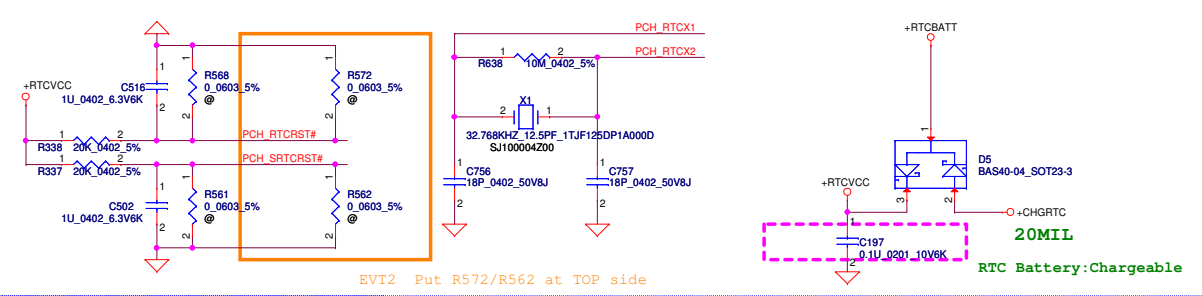
DDR_B_DQS#[0..7]	6
DDR_B_DQS[0..7]	6
DDR_B_D[0..63]	6
DDR_B_MA[0..15]	6

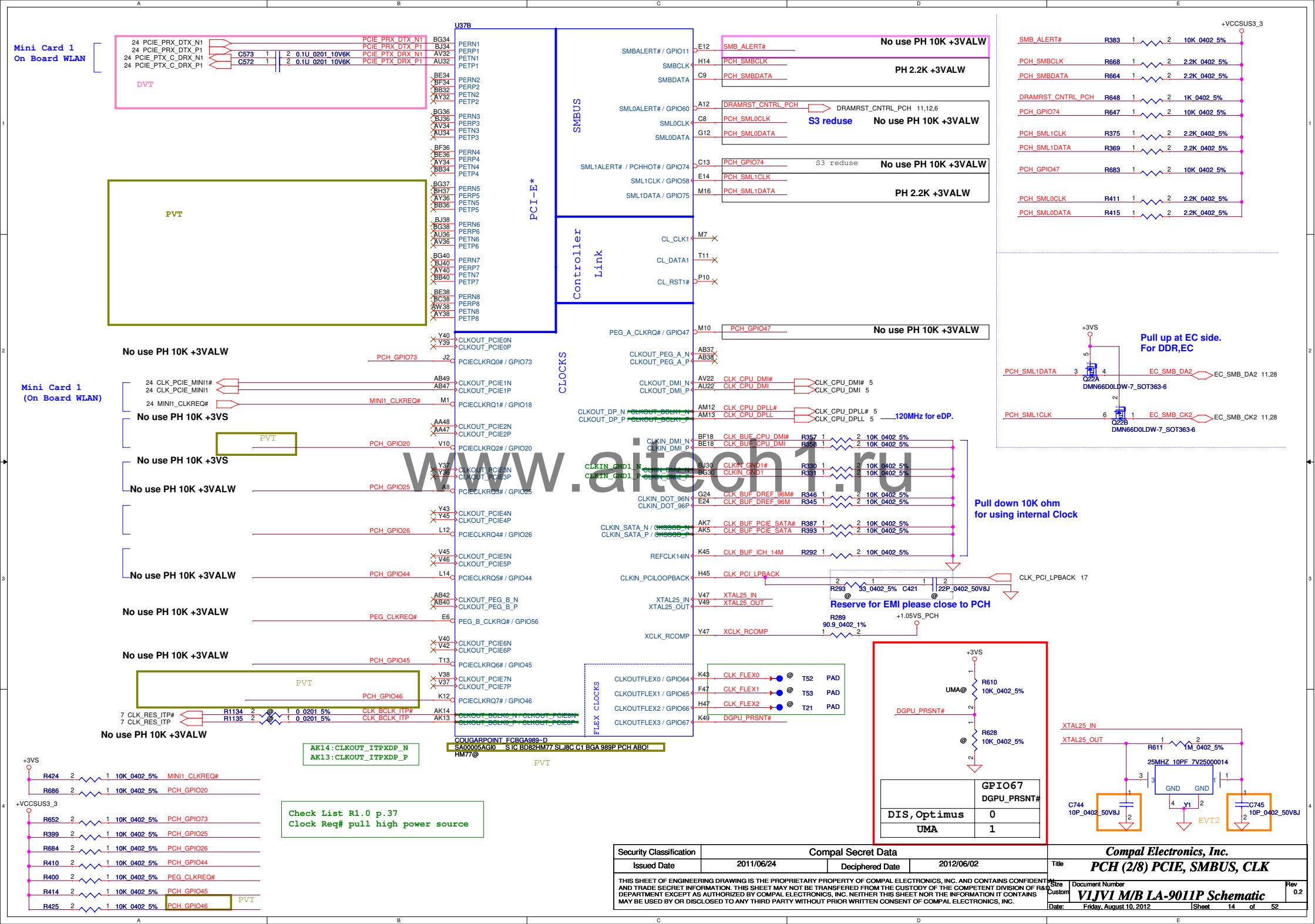


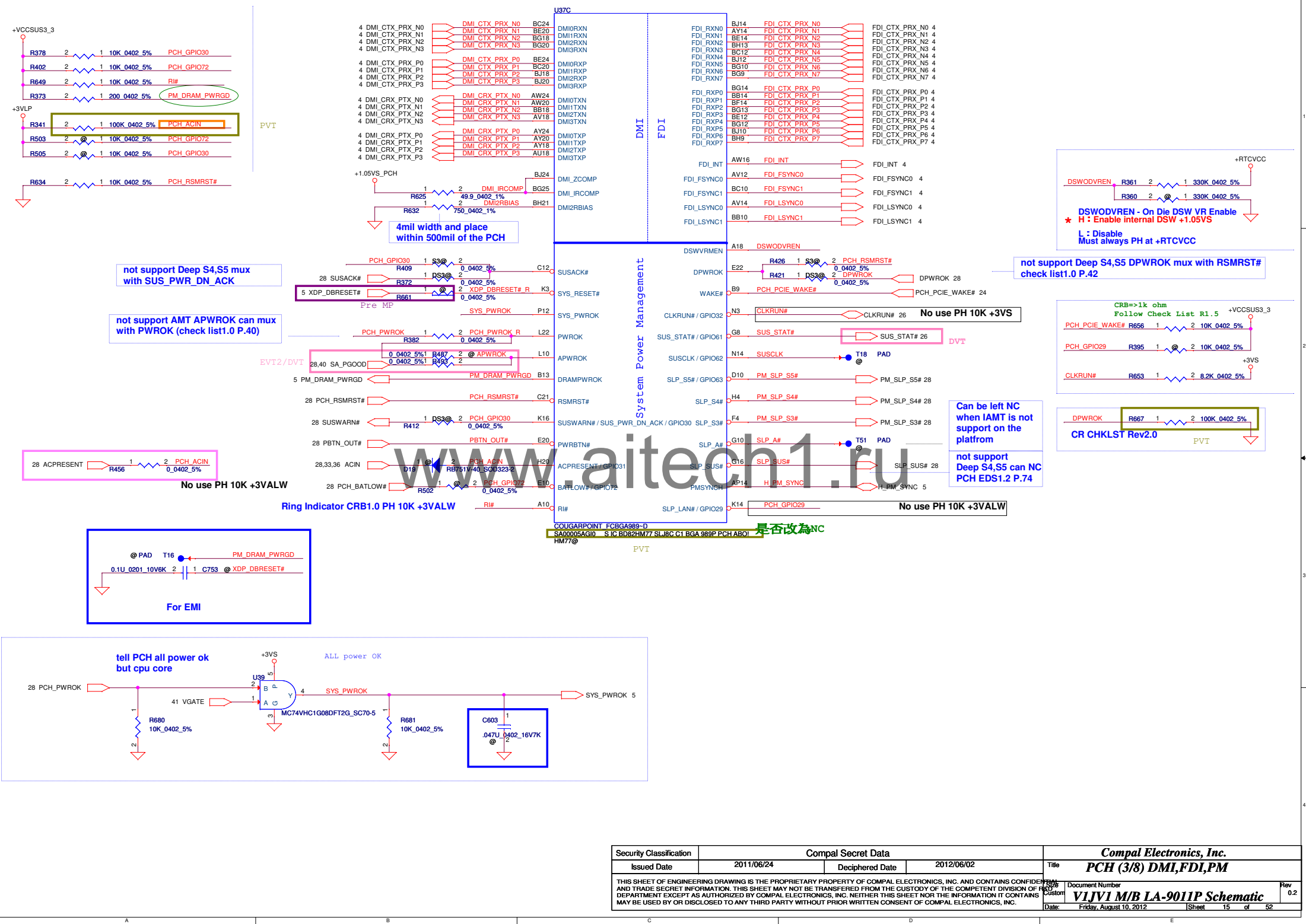
```
Delete U71 SPD EEROM circuit
SA00004KS00
S IC EE 2K AT24C02C-XHM-T TSSOP 8P
```

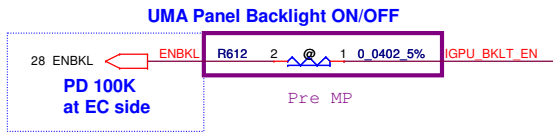


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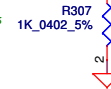


Delete LVDS function

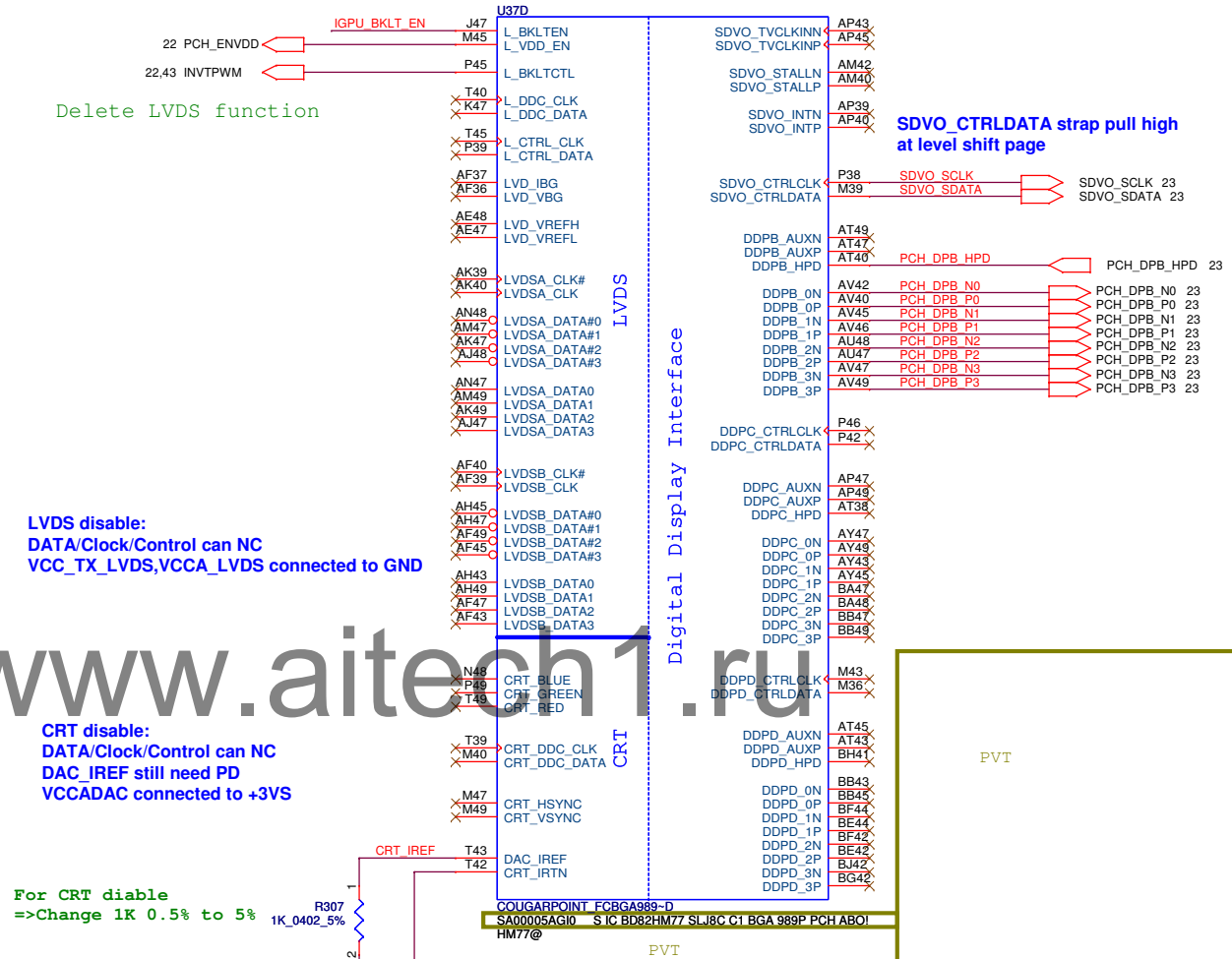
LVDS disable:
DATA/Clock/Control can NC
VCC_TX_LVDS,VCCA_LVDS connected to GND

CRT disable:
DATA/Clock/Control can NC
DAC_IREF still need PD
VCCADAC connected to +3VS

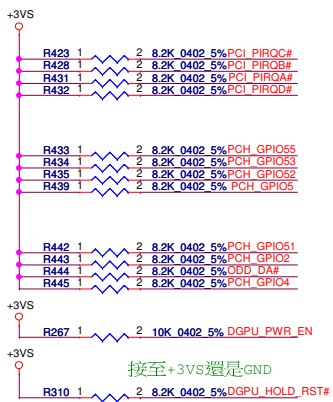
For CRT diable
=>Change 1K 0.5% to 5%



www.aitech1.ru



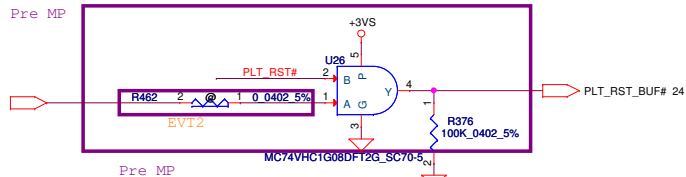
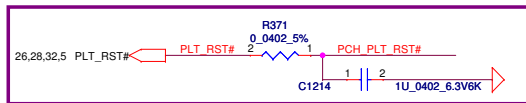
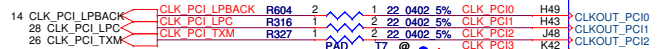
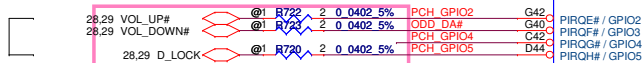
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Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	PCH (4/9) LVDS,CRT,DP,HDMI
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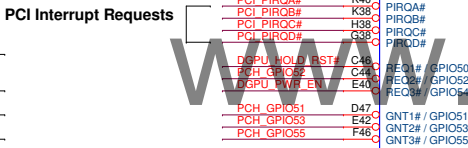
Boot BIOS Strap			
GNT1#/ GPIO51	GPIO19 GPIO51		Boot BIOS
	Bit11	Bit10	Destination
Internal	0	1	Reserved
PH	1	0	PCI
	1	1	SPI
	0	0	LPC

只剩GPIO的功能沒有strap function
不做GPIO要PH +3V5,如做GPIO PH +3V5

只剩GPIO的功能沒有strap function
無須PH(Internal PH),如做GPIO PH +3V5



Sideband signal for Touch screen



COUGARPOINT FCBGA989-D
SA00005AGIO S IC BD82HM77 SL18C C1 BGA 989P PCH ABOI
HM77@

PCI

NVRAM

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

RSVD

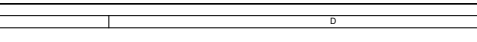
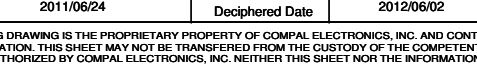
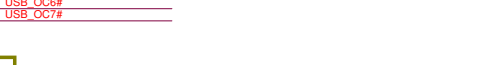
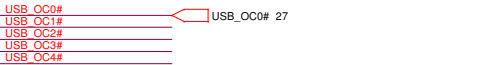
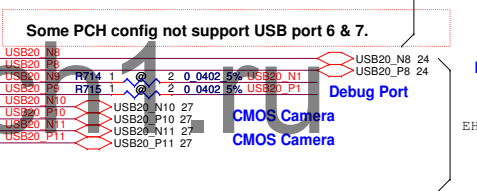
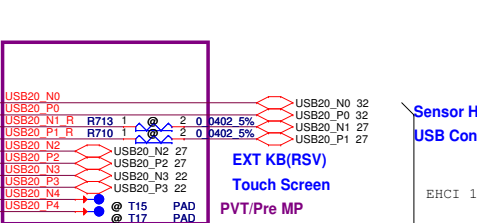
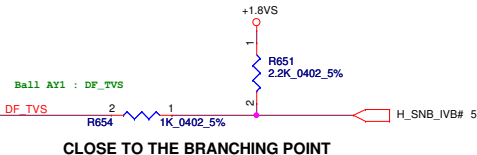
RSVD

RSVD

RSVD

DMI,FDI Termination Voltage	
DF_TV5	Set to Vcc when HIGH
	Set to Vss when LOW

DG1.2 CRB1.0 PH 2.2K series 1K
For 2012 support



Sensor Hub
USB Connector

Bluetooth

Debug Port

CMOS Camera

CMOS Camera

CMOS Camera

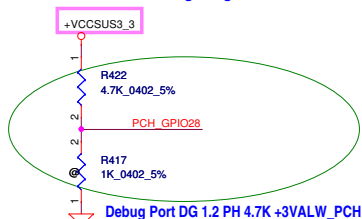
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
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								PCH (5/9) PCI, USB, NVRAM			
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								VIJVI M/B LA-9011P Schematic		0.2	
								Date: Friday, August 10, 2012		Sheet 17 of 52	

HDA_SYNC PH(PLL =+1.5VS)

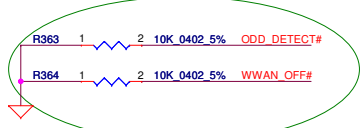
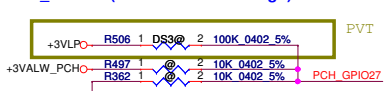
GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up
 * H : On-Die PLL voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal RTC alarm,Power BTN,GPIO27 PCH_GPIO27 (Have internal Pull-High)

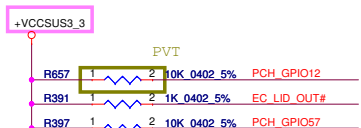
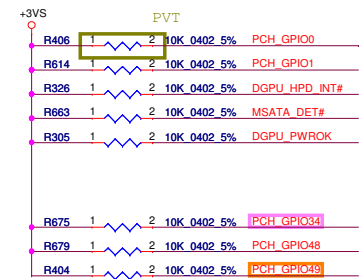


SATA2GP/GPIO36,SATA3GP/GPIO37

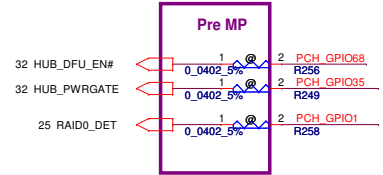
1.Used as for Mechanical Presence detect -
 Use a weak external pull-up (150K-200K Ohms) to Vcc3_3
 or use 10K external pull-up that is enabled only
 after PLTRST# de-assertion.

2.Used as GP Input (Pin HW default) -
 Ensure GPI is not driven high during strap sampling window

3.Unused as GPIO or SATA*GP -
 Use 8.2K-10K pull-down to ground.



GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration
 register bits are not cleared by
 CF9h reset event.
 CRB1.0 PH10K to +3VALW



No use PH 10K +3VS	PVT	PCH_GPIO00	T7
No use PH 10K +3VS		PCH_GPIO01	A42
No use PH 10K +3VS		DGPU_HPD_INT#	H36
	28 EC_SCI#	EC_SCI#	E38
	28 EC_SMI#	EC_SMI#	C10

No use PH +3VALW	PVT	PCH_GPIO12	C4
No use PH +3VALW	EC LID SW OUT	EC_LID_OUT#	G2
No use PH +3VS	25 MSATA_DET#	MSATA_DET#	U2

No use PH 10K +3VS		PCH_GPIO22	D40
CRB1.0 PH 10K +3VALW		PCH_GPIO24	E8
No use PD 10K to GND	28 EC_DS3_WAKE#	PCH_GPIO27	E16
No use PH 10K +3VALW		PCH_GPIO28	P8
No use PH 10K +3VS		PCH_GPIO34	K1
No use can NC(+3VS power plane)		PCH_GPIO35	K4
Can't PH		ODD_DETECT#	V8
Can't PH		WWAN_OFF#	M5
No use PH 10K +3VS Optimus(L)/ non optimus(H)		OPTIMUS_EN#	N2
No use PH 10K +3VS		PCH_GPIO39	M3
No use PH 10K +3VS		PCH_GPIO45	V49
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS	PVT	PCH_GPIO49	V3
No use PH +3VALW		PCH_GPIO57	O6

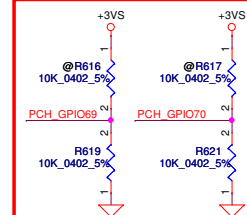
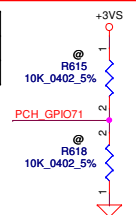
	GPIO38 OPTIMUS_EN#
Muxless	0
nonMuxless	1

Define Q5LJ1 (DDR3) or V1JV1 (DDR3L)

	GPIO24 PCH_GPIO24
DDR3L(V1JV1)	0
DDR3	1

GPIO36/GPIO37 is Strap functionality
 that requires internal pull down to be sampled at rising PWROK.
 When uses as SATA2GP/SATA3GP for mechanical presence detect
 -use a external pull up 150K-200K ohm to Vcc3_3
 When used as GP input
 -ensure GPI is not driven high during strap sampling window
 When Unused as GPIO or SATA*GP
 -use 8.2K-10K pull-down
 check list page 47

LVDS/eDP	GPIO71
LVDS	1
eDP	0



SW base on TPM table to detect HW TPM status

TPM Status	GPIO69	GPIO70
HW, SW without support TPM	0	0
HW, SW support TPM (1.2)	0	1
HW, SW support TPM (2.0)	1	0
x	1	1

GPIO

CPU/MISC

NC/F

VSS/NCTF

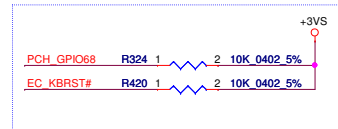
DVT

PVT

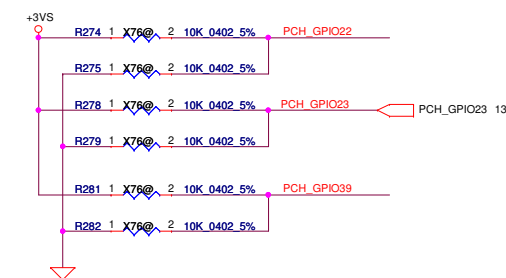
Remove NCTF test point
 2011/9/23

INIT3_3V Check list1.0 P.59
 This signal has weak internal
 PU, can't pull low,leave NC

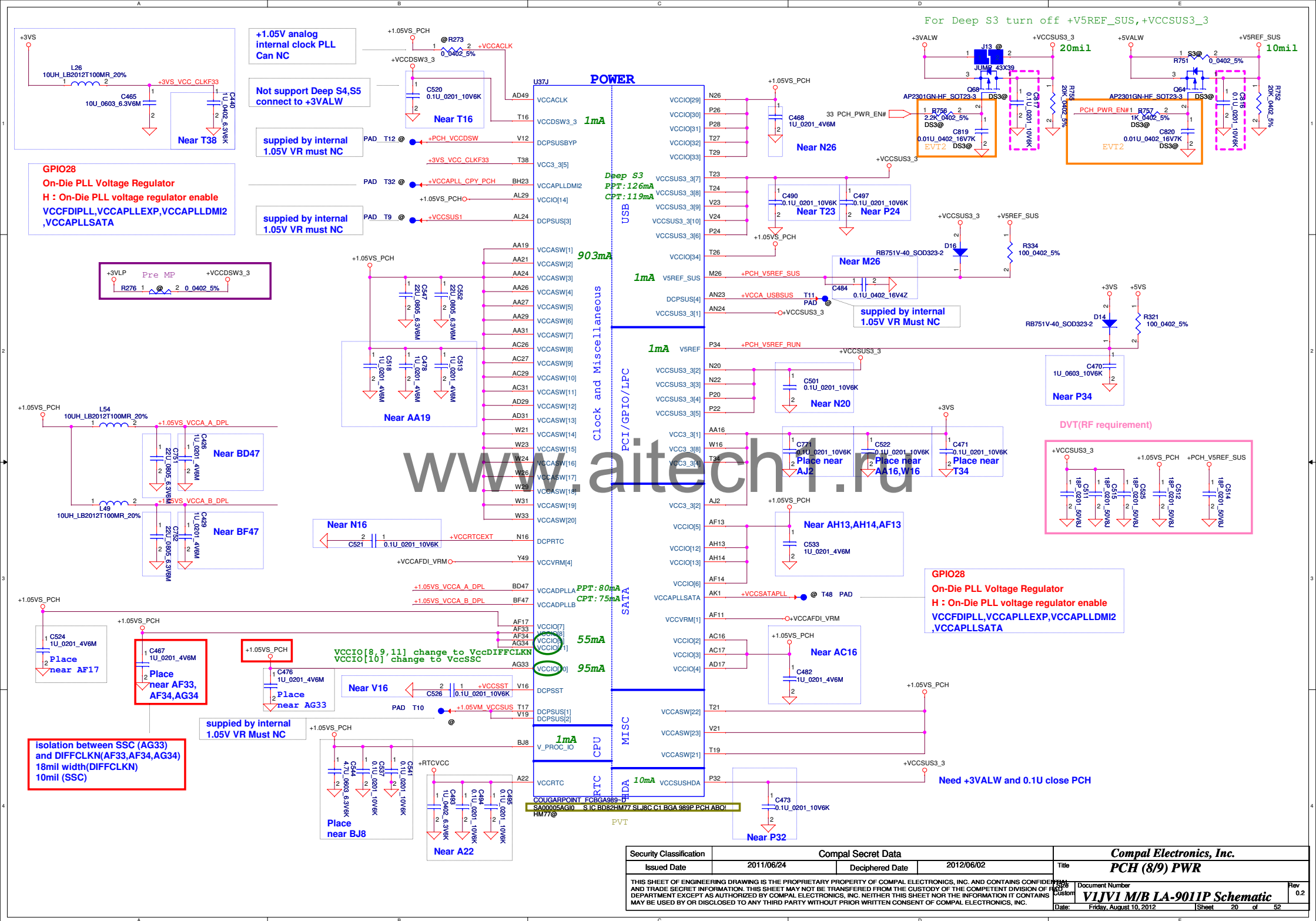
TS_VSS1~4
 PD to GND

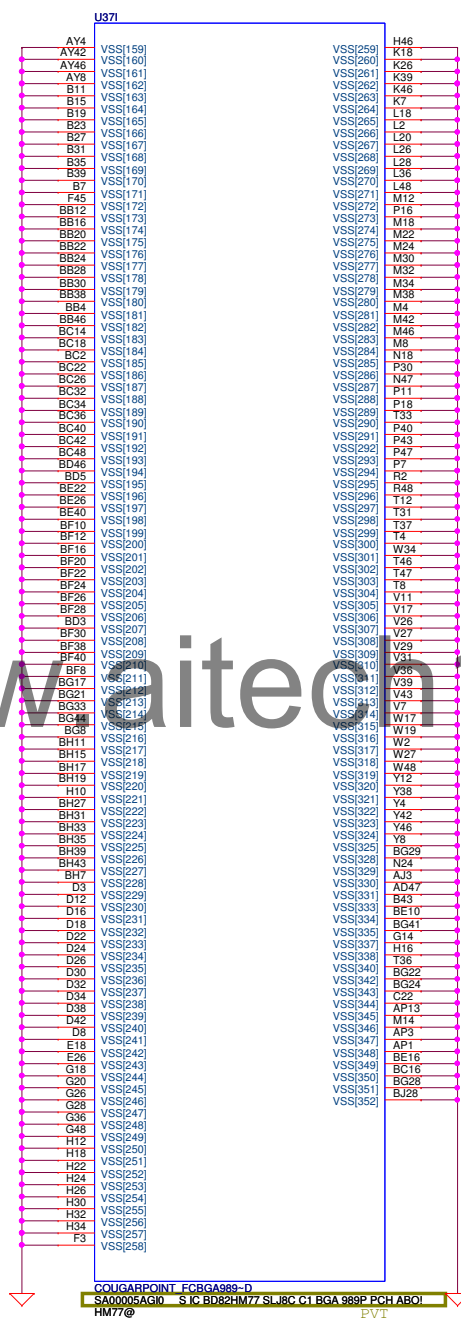
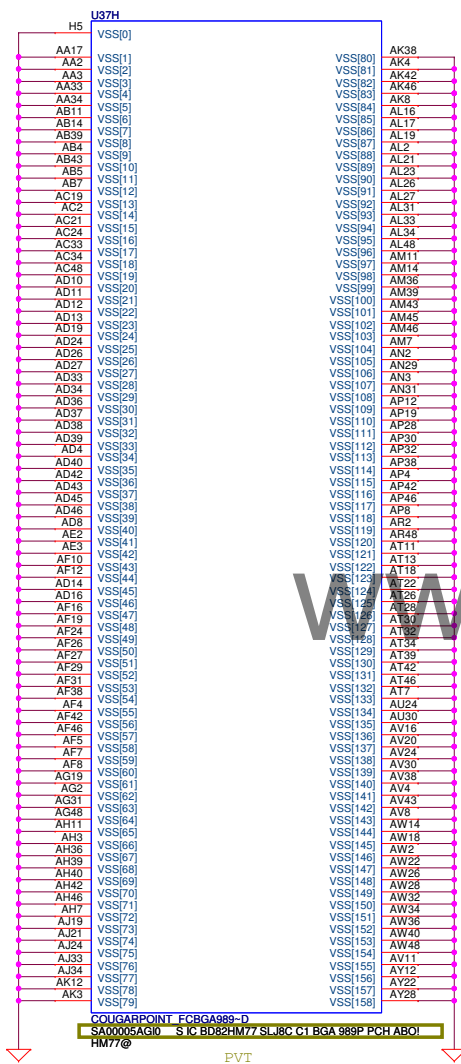


	GPIO39	GPIO23	GPIO22
Elpida Mono 512MB*4 (Ch A)	0	0	0
Hynix Mono 512MB*4 (Ch A)	0	0	1
Elpida Mono 512MB*8 (Ch A,B)	0	1	0
Hynix Mono 512MB*8 (Ch A,B)	0	1	1



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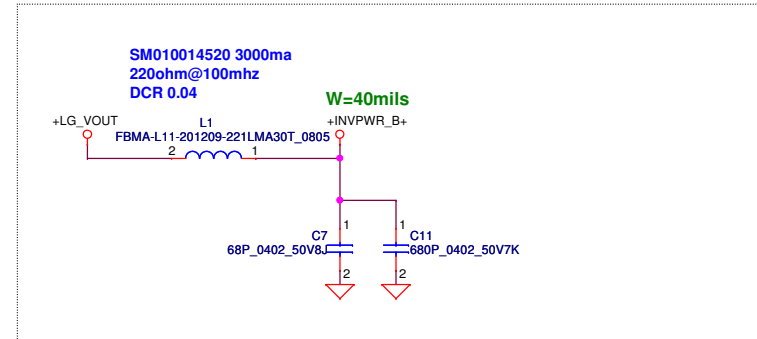
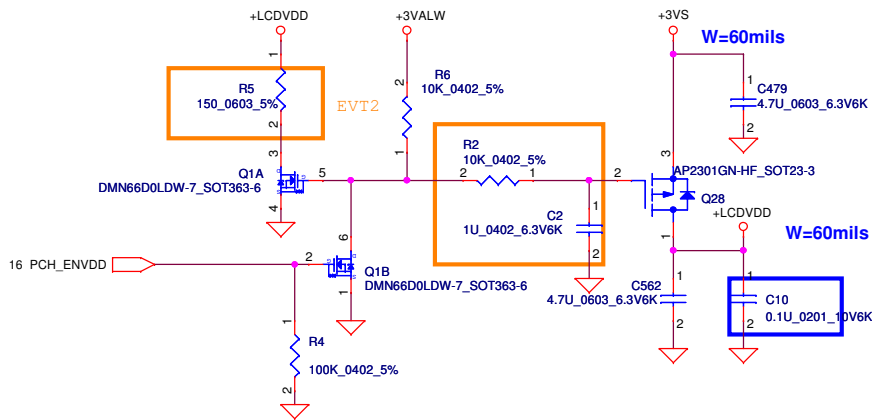




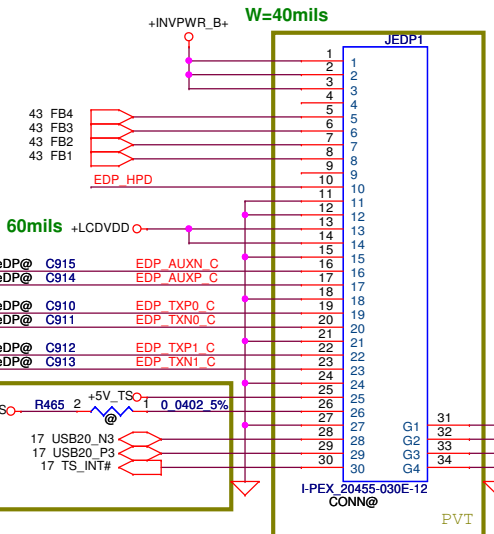
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Issued Date		2011/06/24	Deciphered Date	2012/06/02	Title
					PCH (9/9) VSS
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Compal Electronics, Inc.
PCH (9/9) VSS

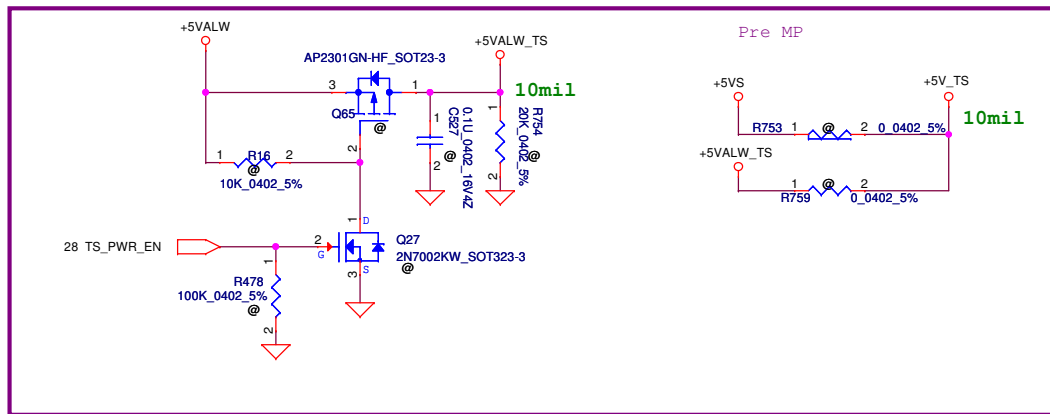
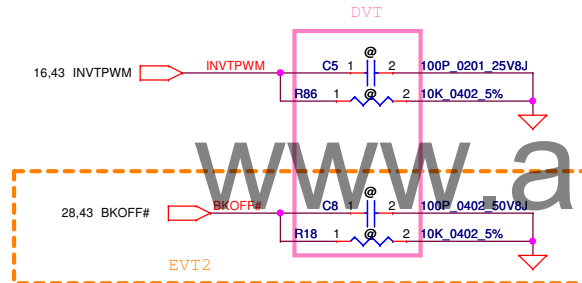
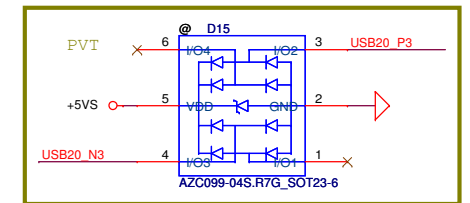
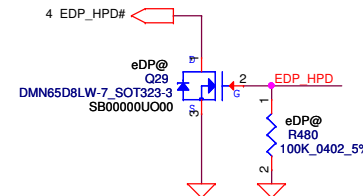
Panel POWER CIRCUIT



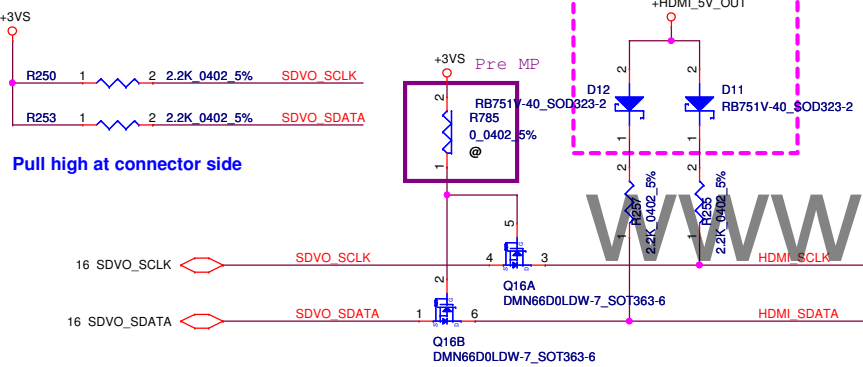
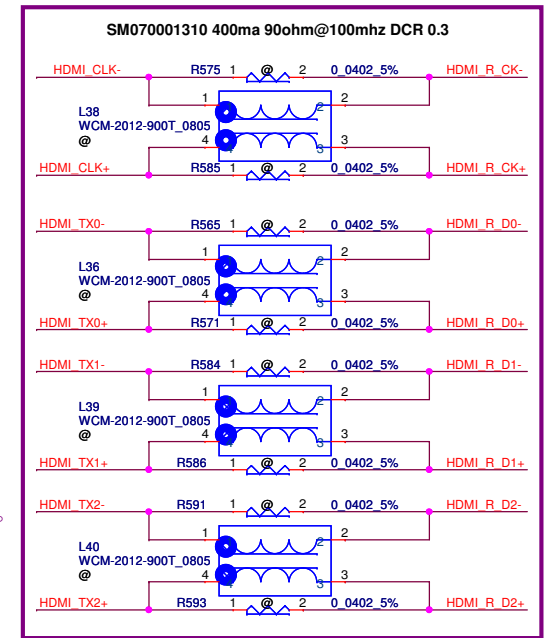
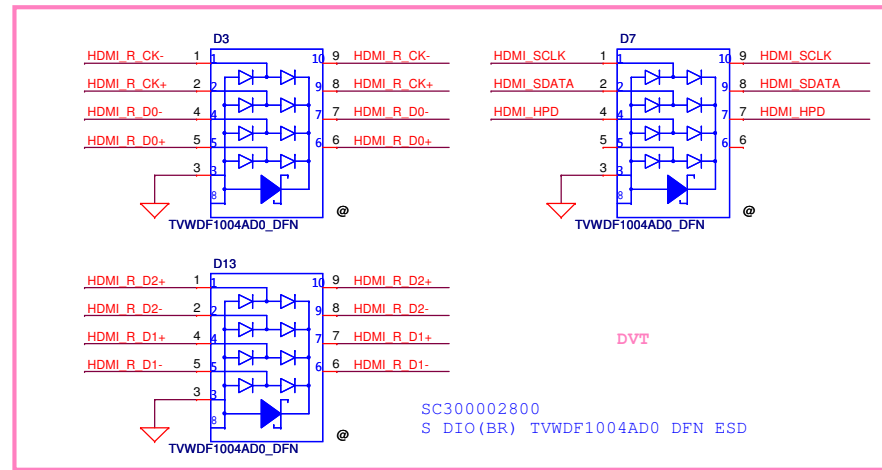
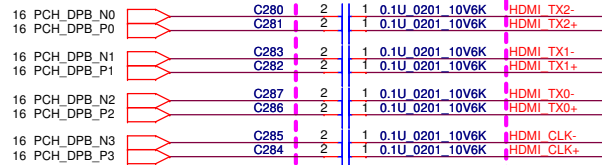
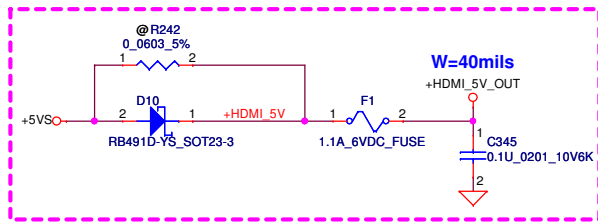
eDP PANEL Conn.



Touch Screen

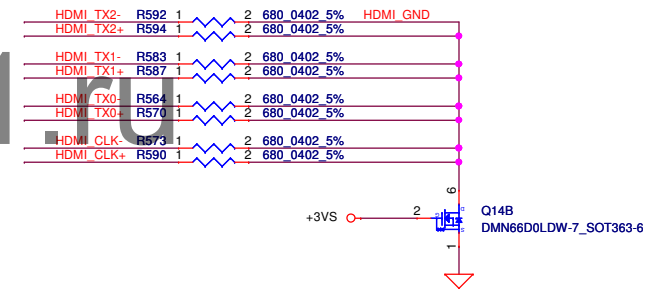
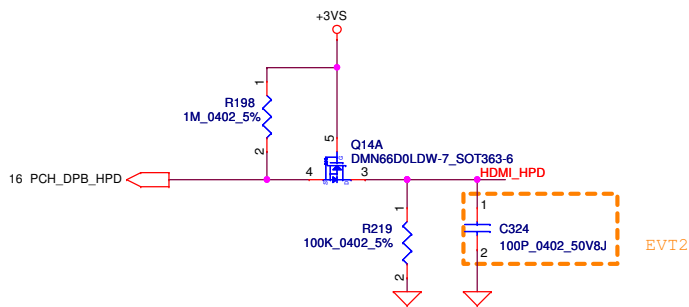


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				Date	Friday, August 10, 2012
				Sheet	22 of 52
				Rev	0.2

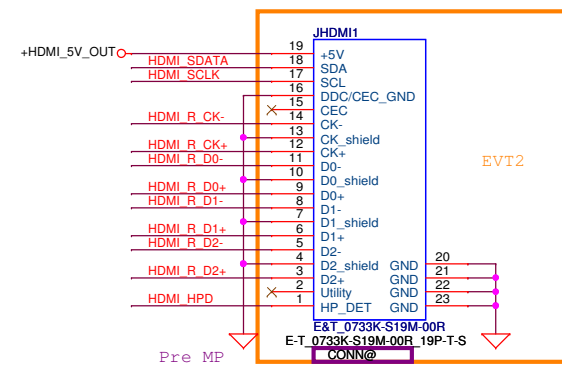


Pull high at connector side

Place closed to JHDMI1



Micro HDMI connector
PCB Footprint : E-T_0733K-S19M-00R_19P-T-S



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Without Support ISCT

60mil

+3VS +3VS_WLAN

J10

JUMP_43X79

1 2

Without Support ISCT

With Support ISCT

+3VS_WLAN

1 2

C403 4.7U_0603_5.3V6K

1 2

C735 0.1U_0201_10V6K

With Support ISCT

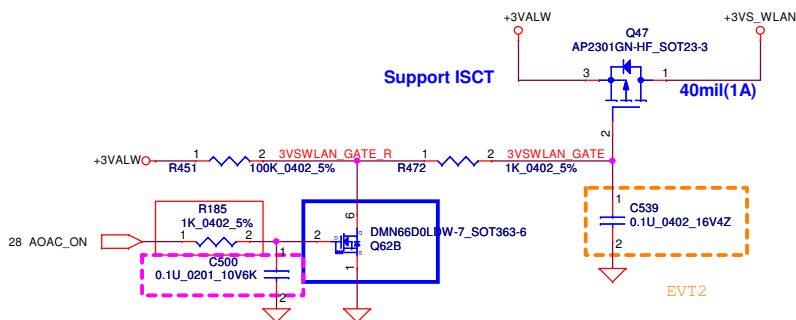
Mini Card Power Rating

+3VS_WLAN

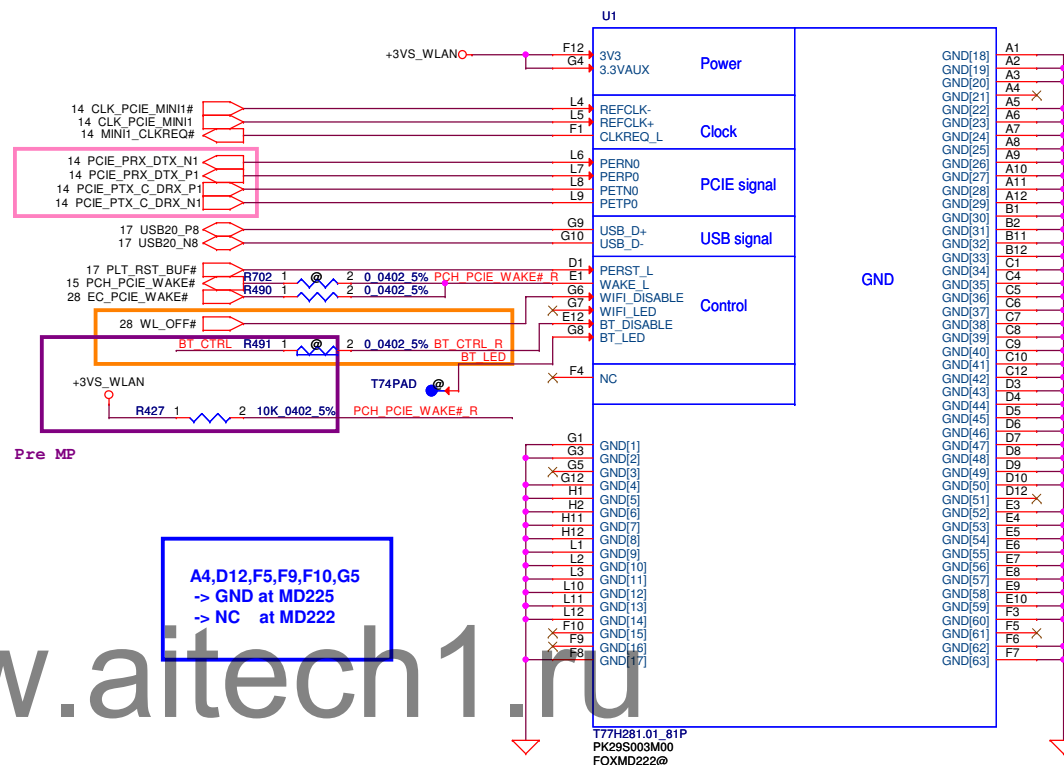
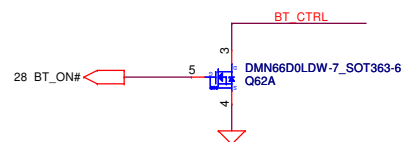
1 2

C387 0.1U_0201_10V6K

Mini Card Power Rating

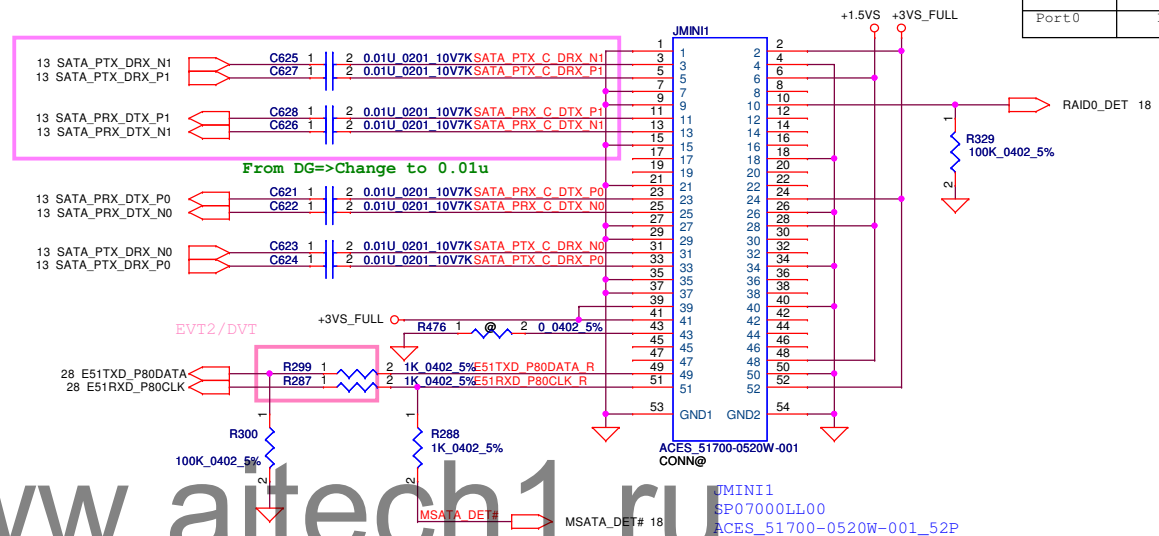
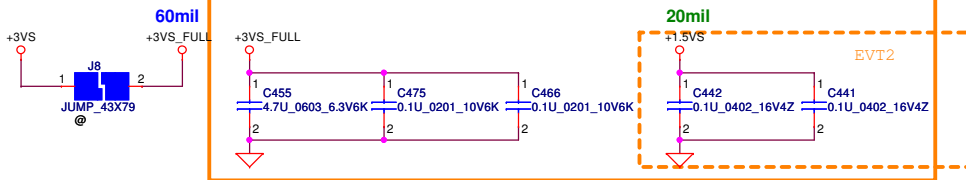


	BT Enable	BT Disable
BT_ON#	L	H
BT_CTRL	H	L



A4,D12,F5,F9,F10,G5
-> GND at MD225
-> NC at MD222

For mSATA

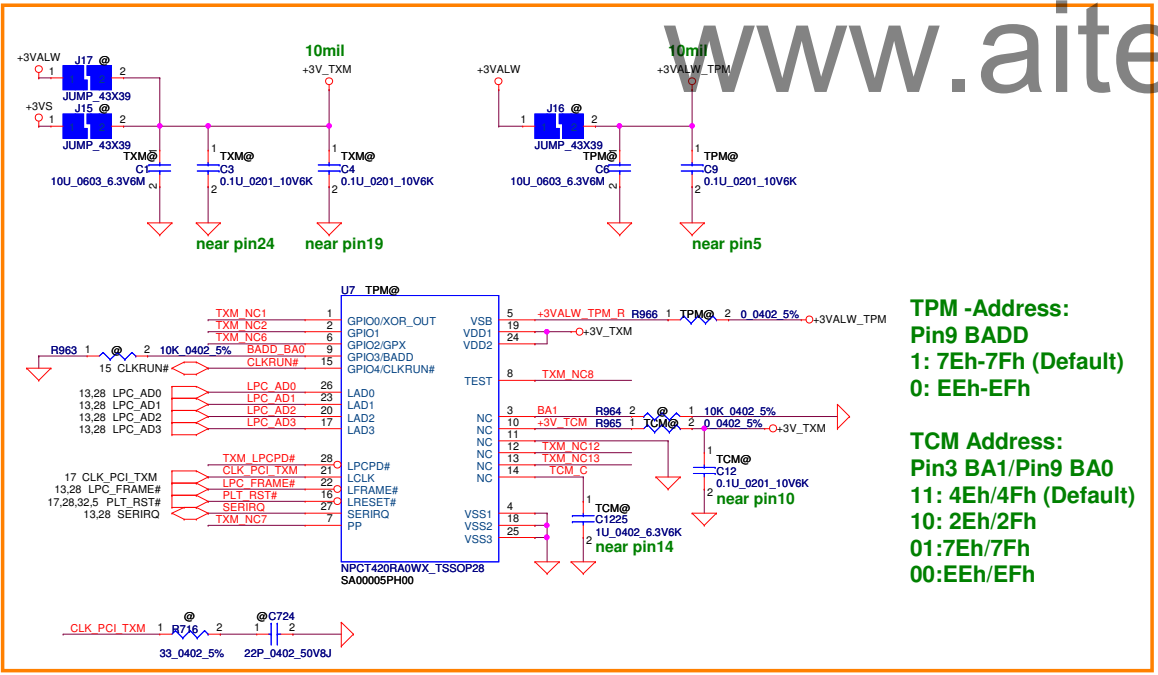


The screenshot shows a network packet capture interface. At the top, a packet is identified as '100K_0402_5%' with a size of 100K. The destination is 'MSATA_DET# 18'. The packet is captured on the 'CONN@' interface. The packet structure is shown with a red arrow pointing to the 'MSATA_DET#' field. The packet is captured on the 'CONN@' interface.

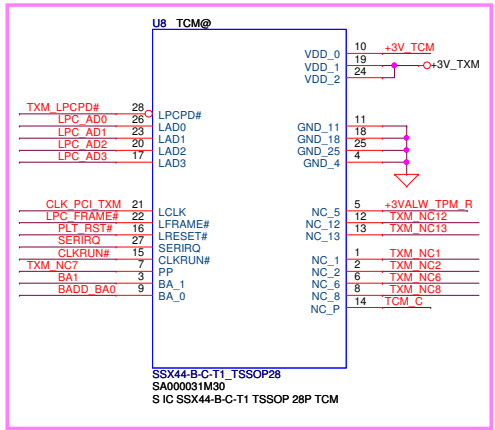
Function	RAID0_DET
Port0,1	H
Port0	L

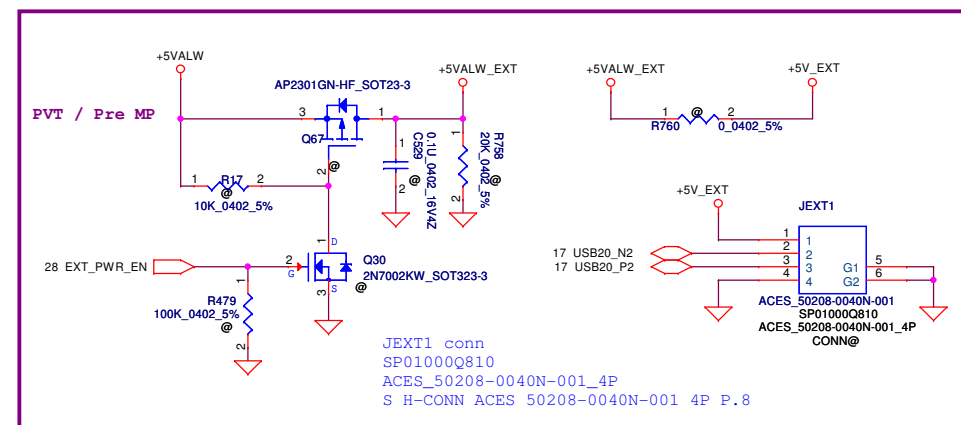
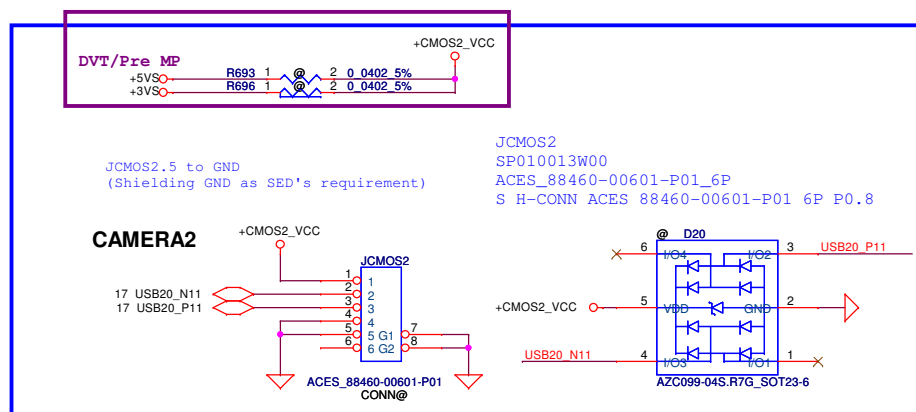
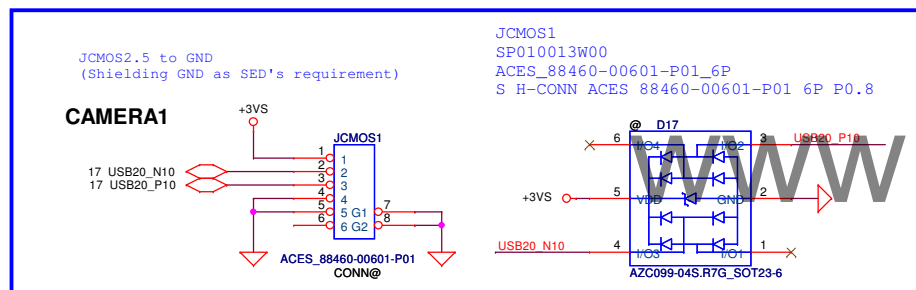
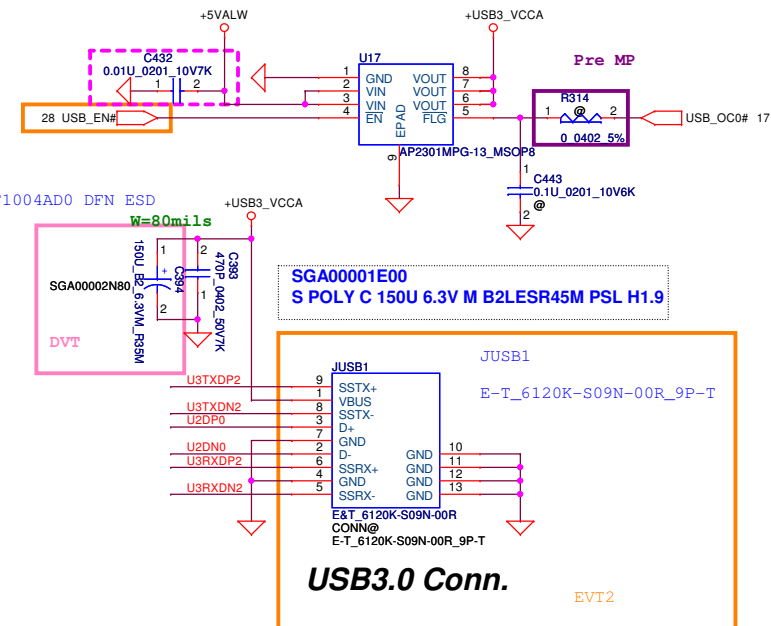
TPM/TCM

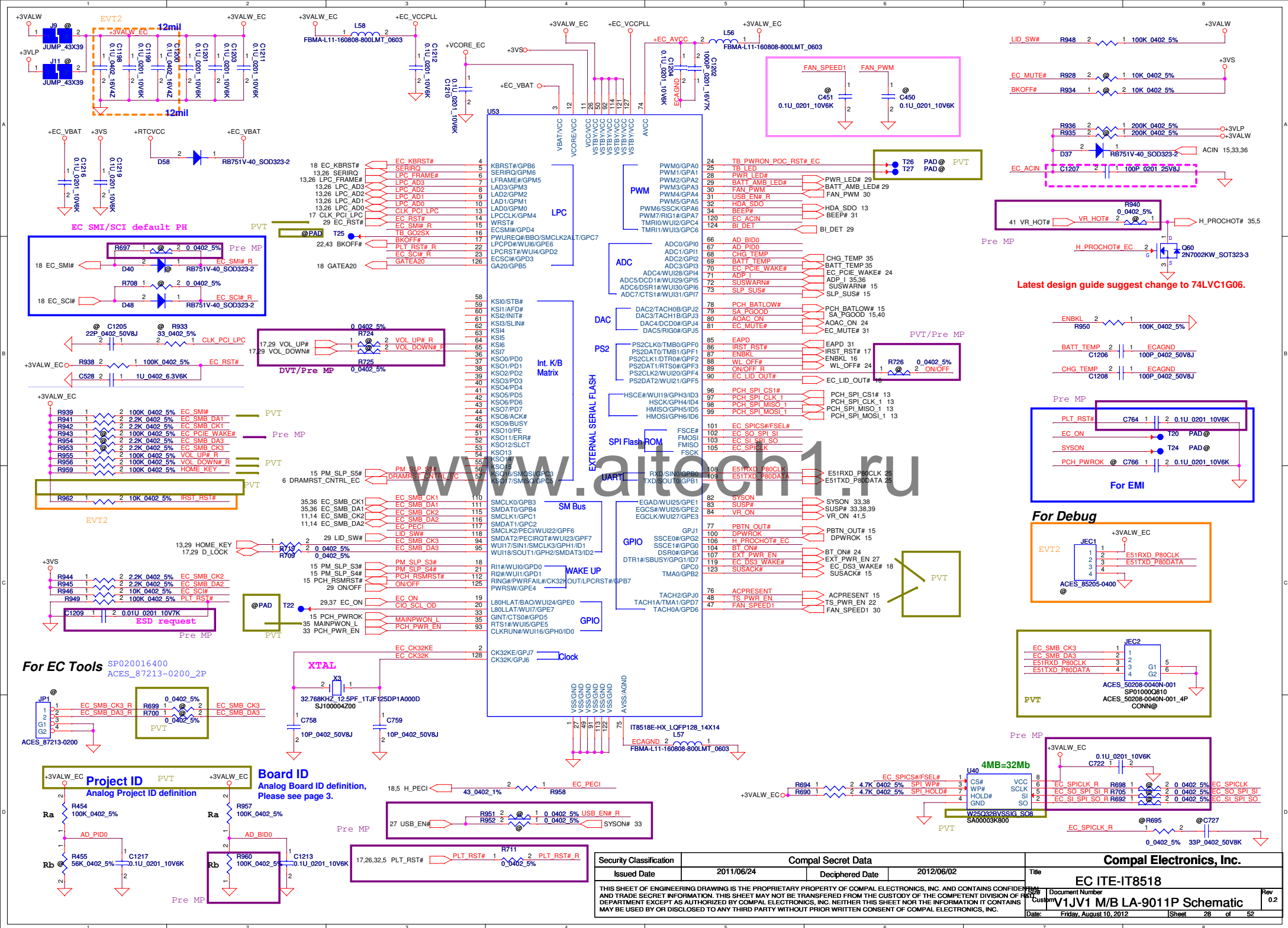
TPM
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S IC NPCT420RA0WX TSSOP 28P TPM

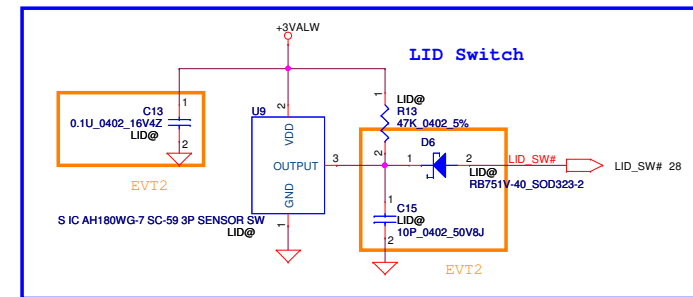
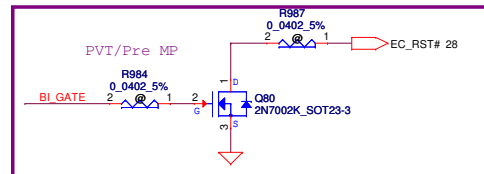
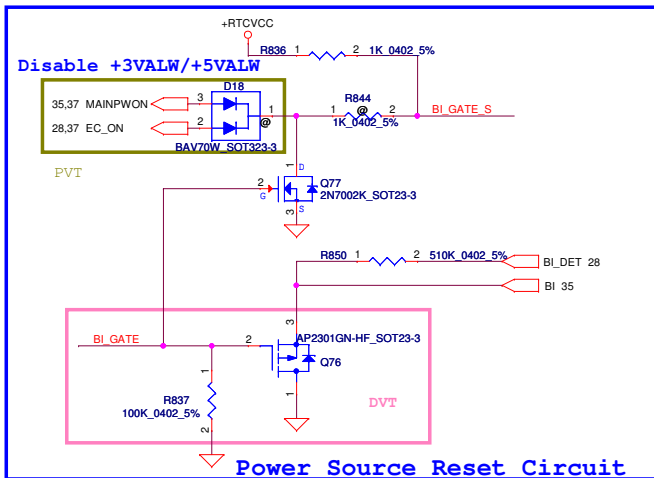
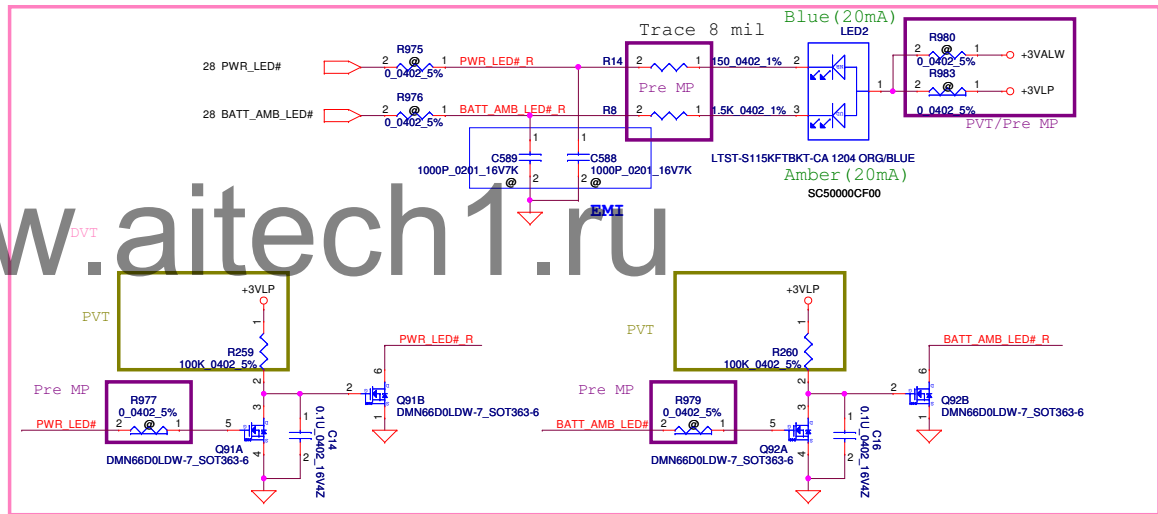
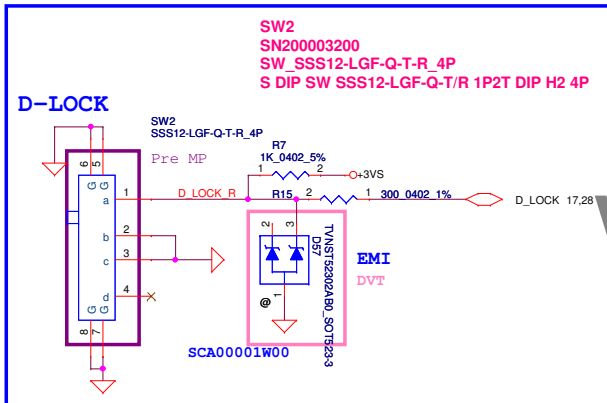
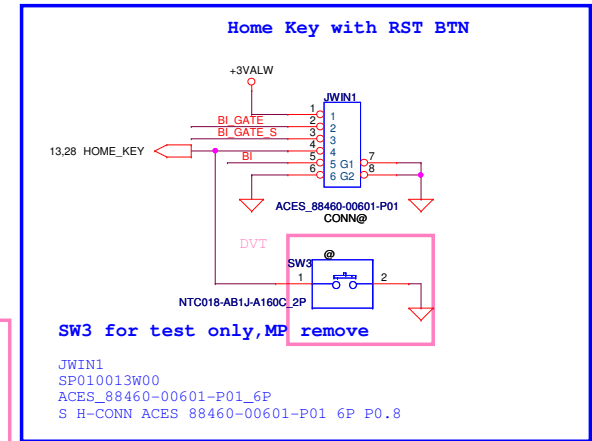
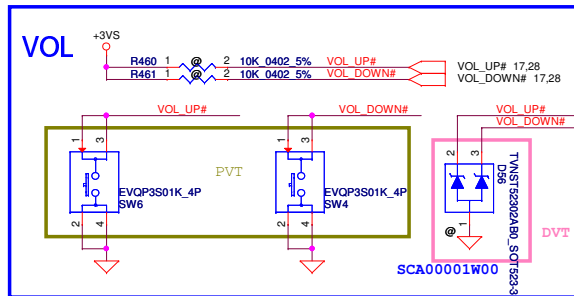
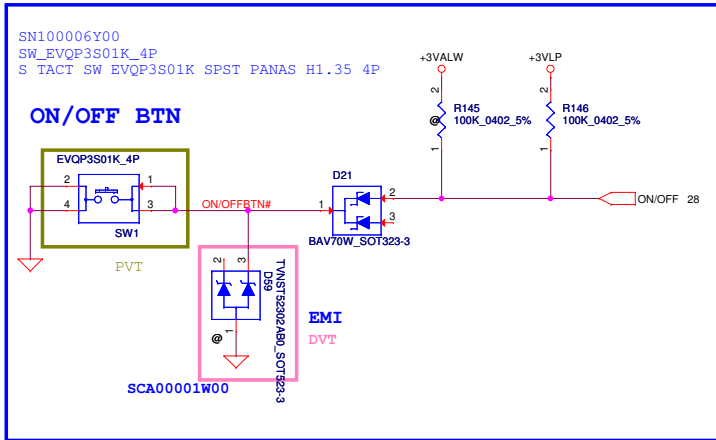


TCM
SA000031M30
S IC SSX44-B-C-T1 TSSOP 28P TCM



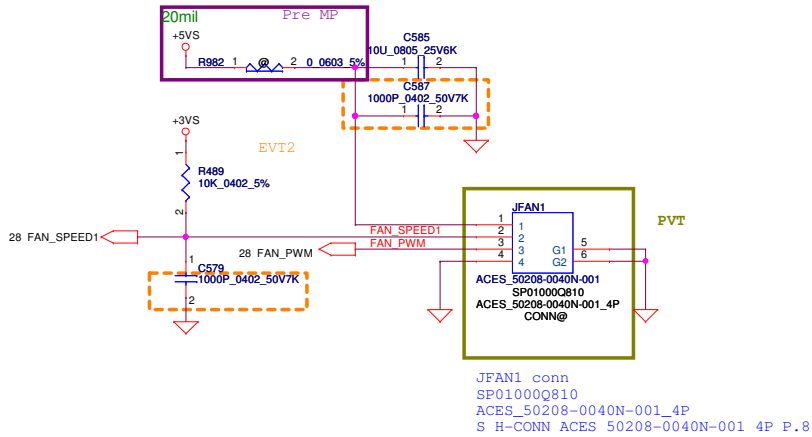






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					Document Number	
					V1JV1 M/B LA-9011P Schematic	
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				Rev 0.2		

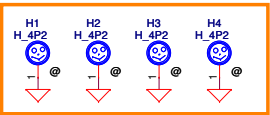
FAN Conn



定位孔



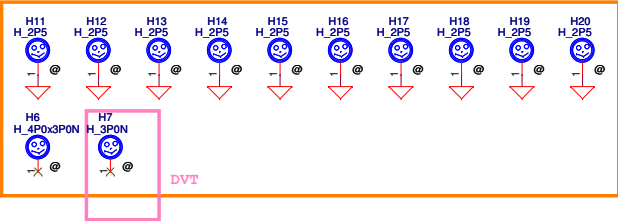
Thermal module



mSATA Stand-Off

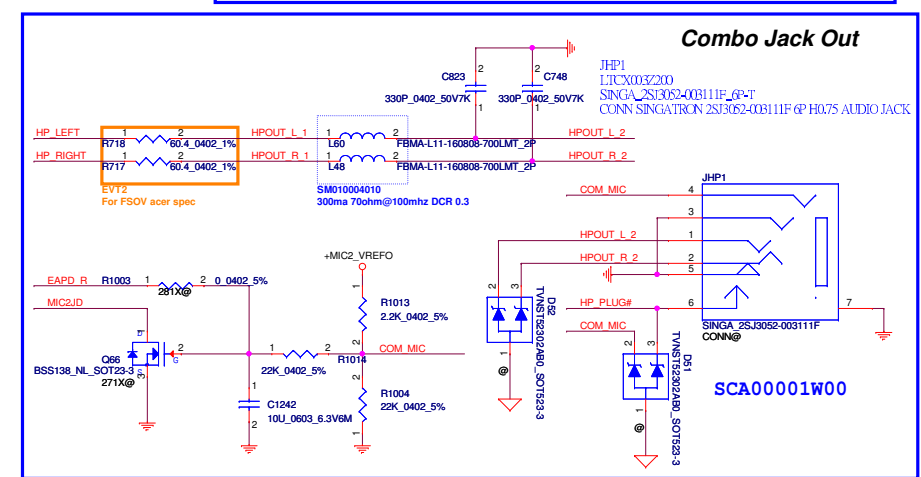
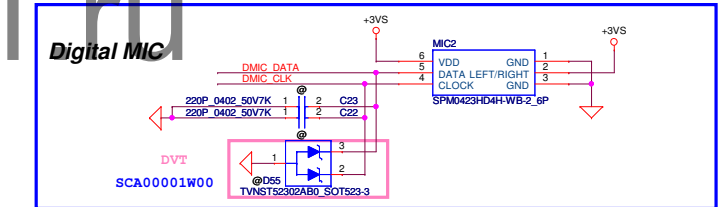
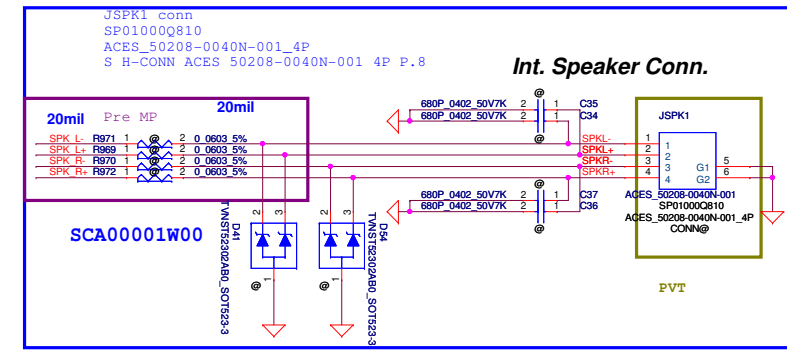
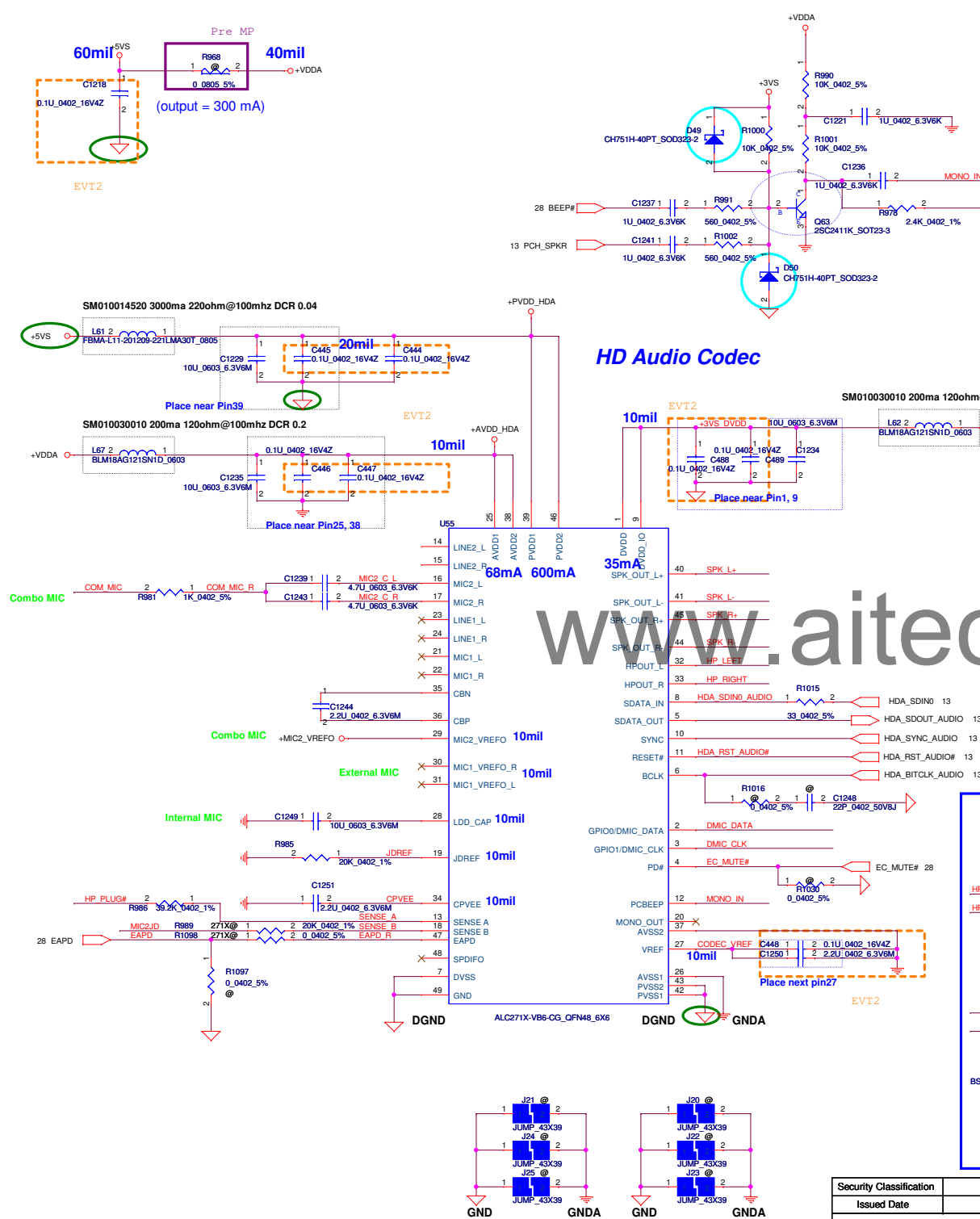


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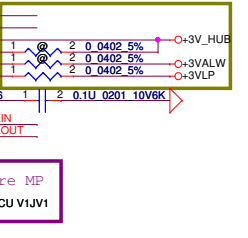
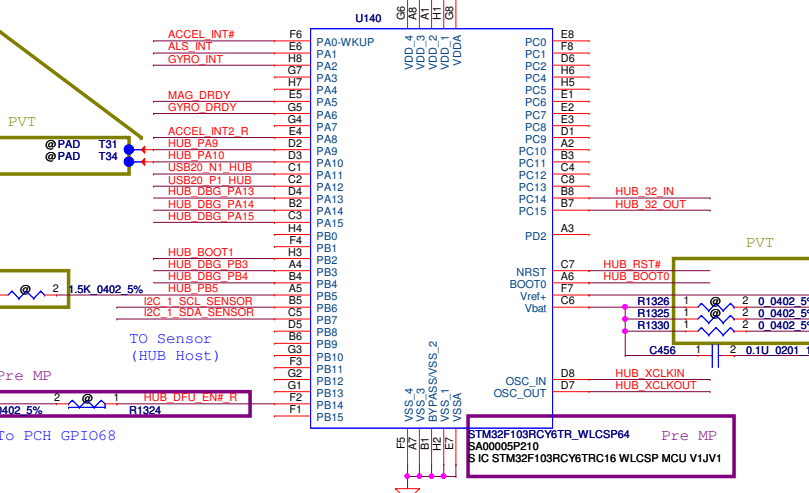
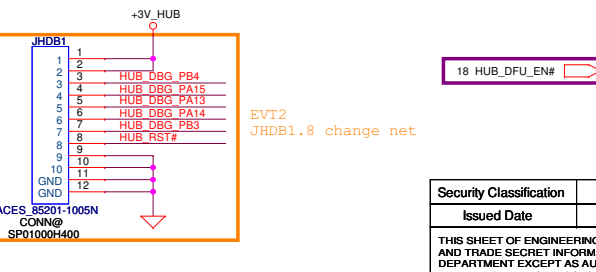
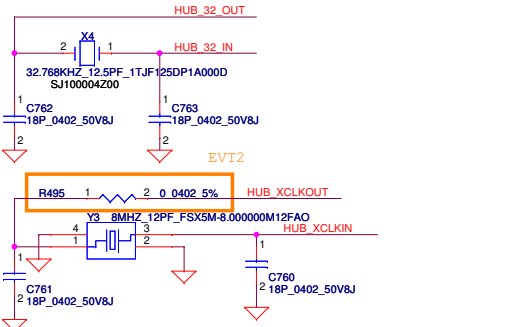
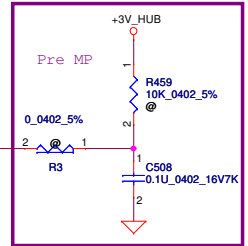
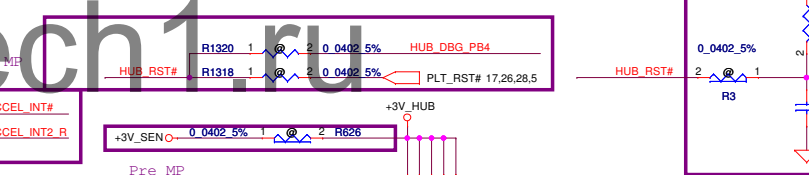
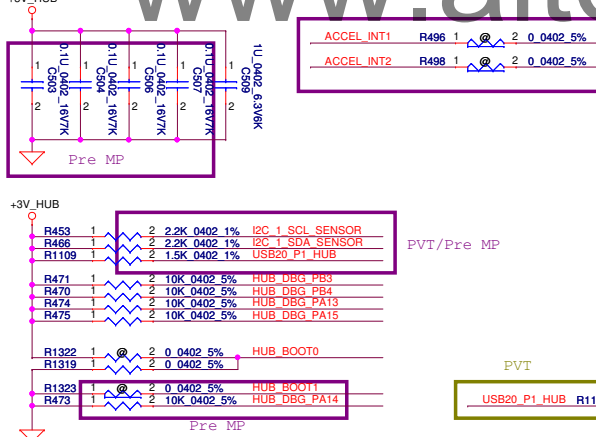
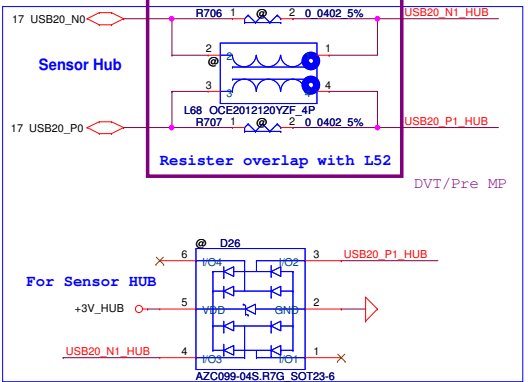
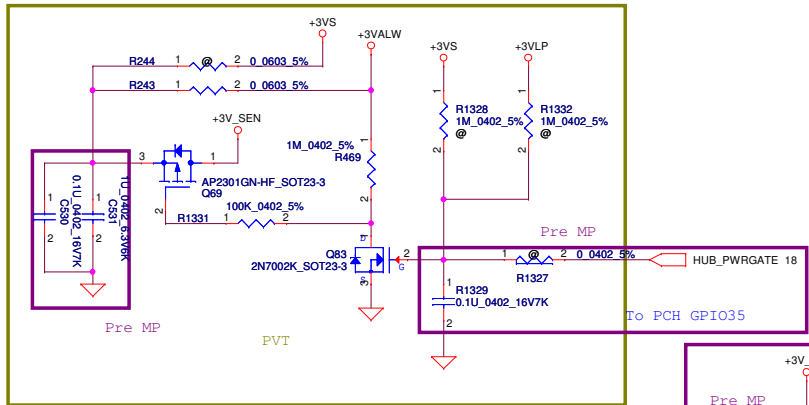
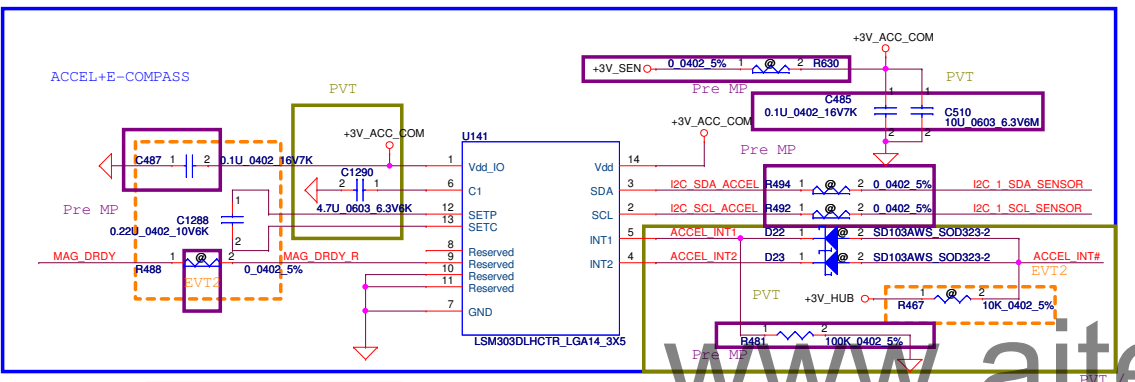
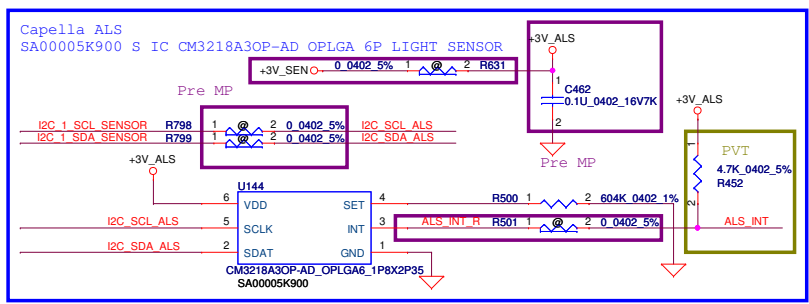
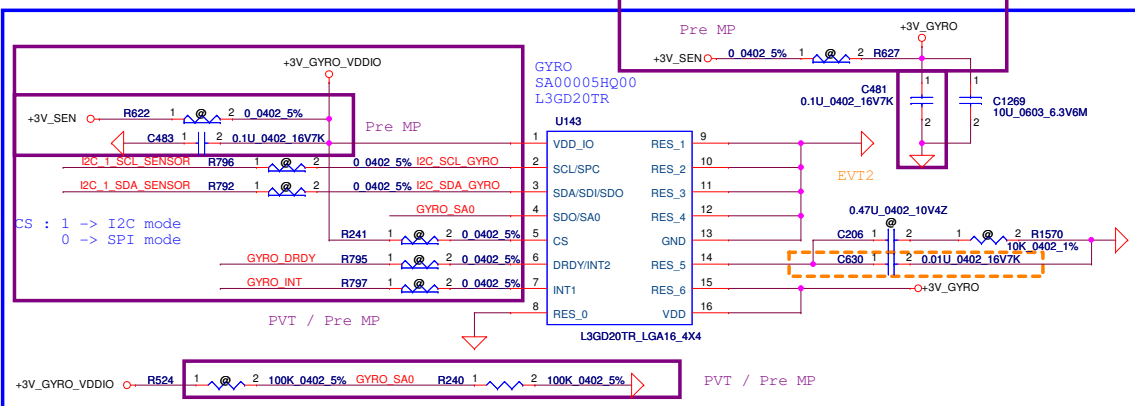


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				V1JV1 M/B LA-9011P Schematic	0.2
				Date: Tuesday, August 14, 2012	Sheet 30 of 52



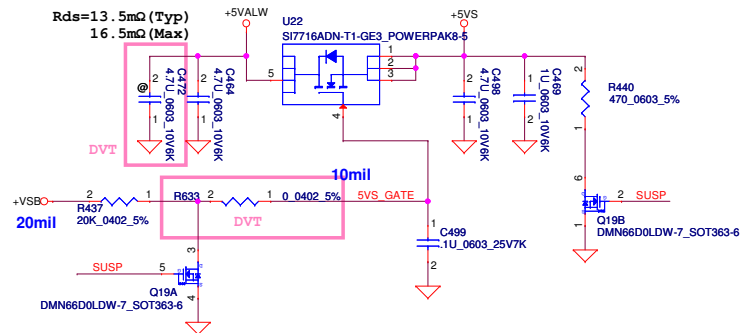
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Issued Date	2010/11/1	Deciphered Date	2011/11/1	Title	
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				V1JY1 M/B LA-9011P Schematic	0.1
				Date: Tuesday, August 14, 2012	Sheet 31 of 32



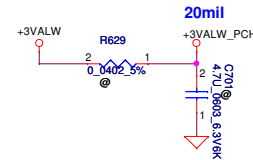
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title	
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				V1Jv1 M/B LA-9011P Schematic	0.1
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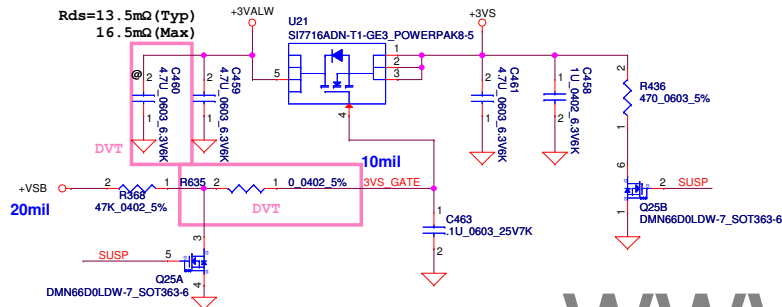
+5VALW to +5VS



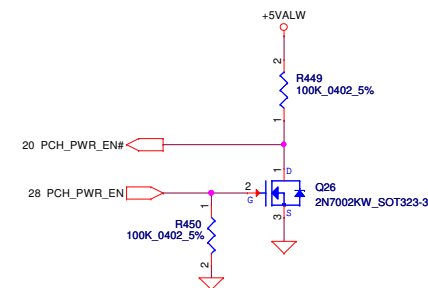
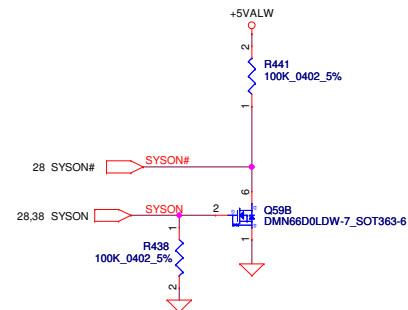
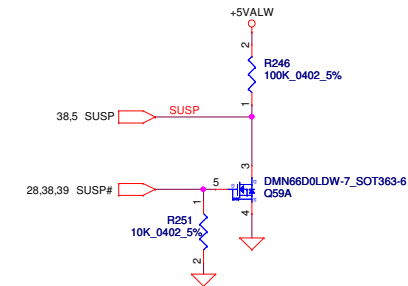
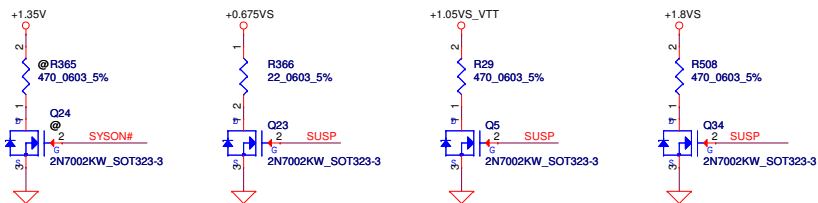
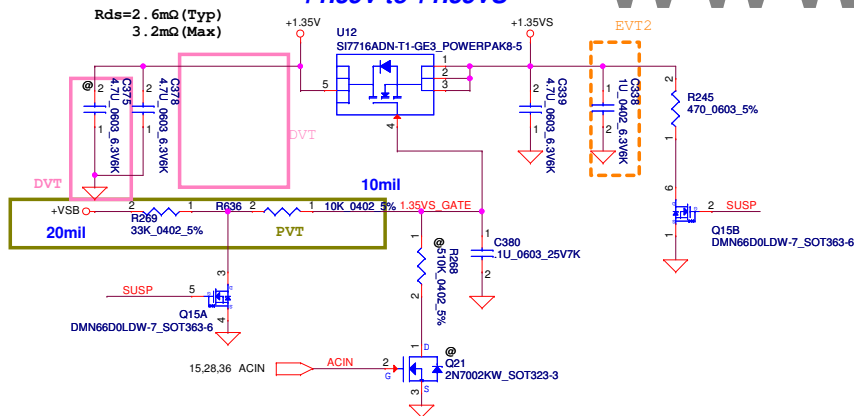
+3VALW to +3VALW_PCH(PCH AUX Power)



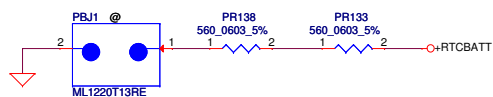
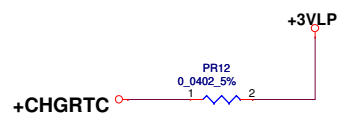
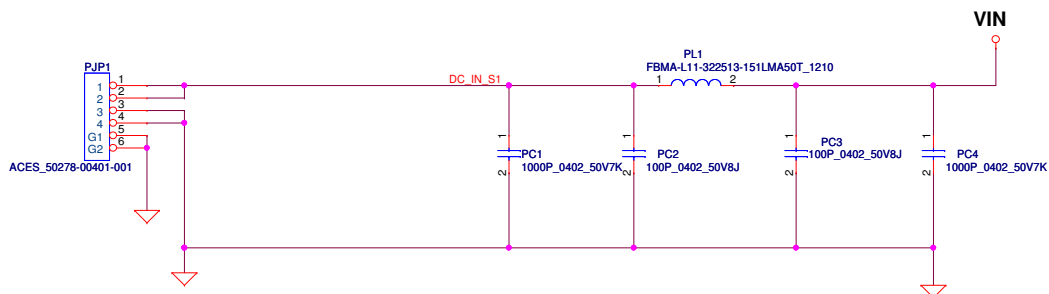
+3VALW to +3VS



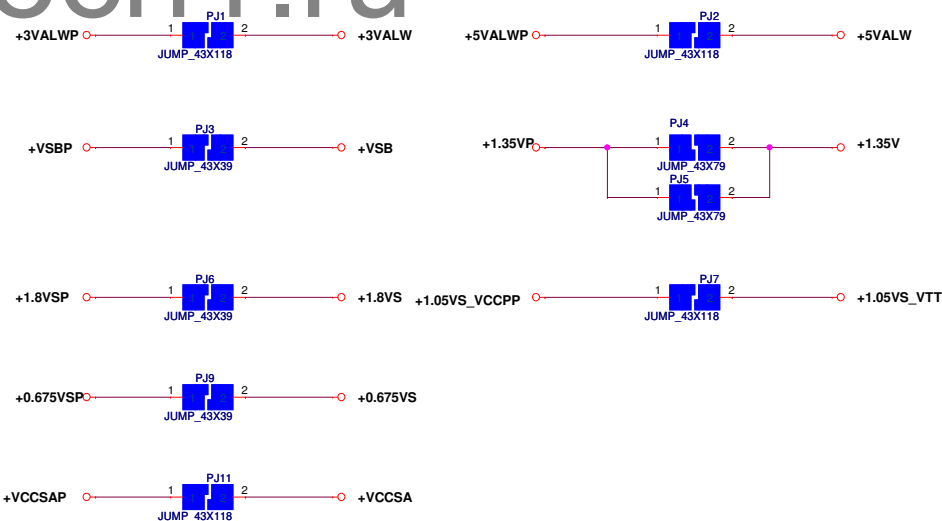
+1.35V to +1.35VS



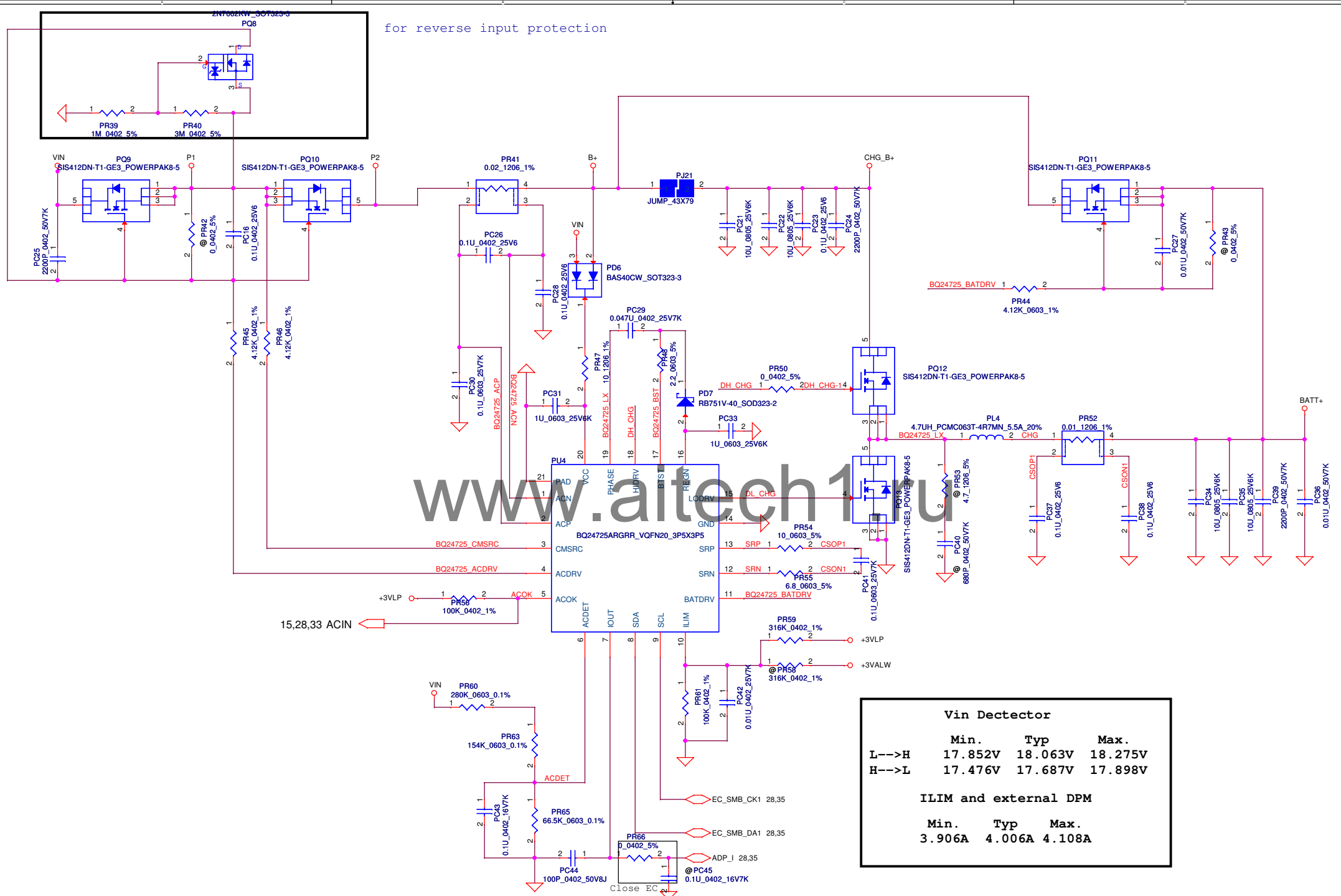
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2011/06/24	Deciphered Date	2012/06/02	Title			
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					Document Number	V1JV1 M/B LA-9011P Schematic	Rev	0.2
					Customer	Friday, August 10, 2012	Sheet	33 of 52
					Date:	Friday, August 10, 2012	Sheet	33 of 52
					Date:	Friday, August 10, 2012	Sheet	33 of 52
					Date:	Friday, August 10, 2012	Sheet	33 of 52



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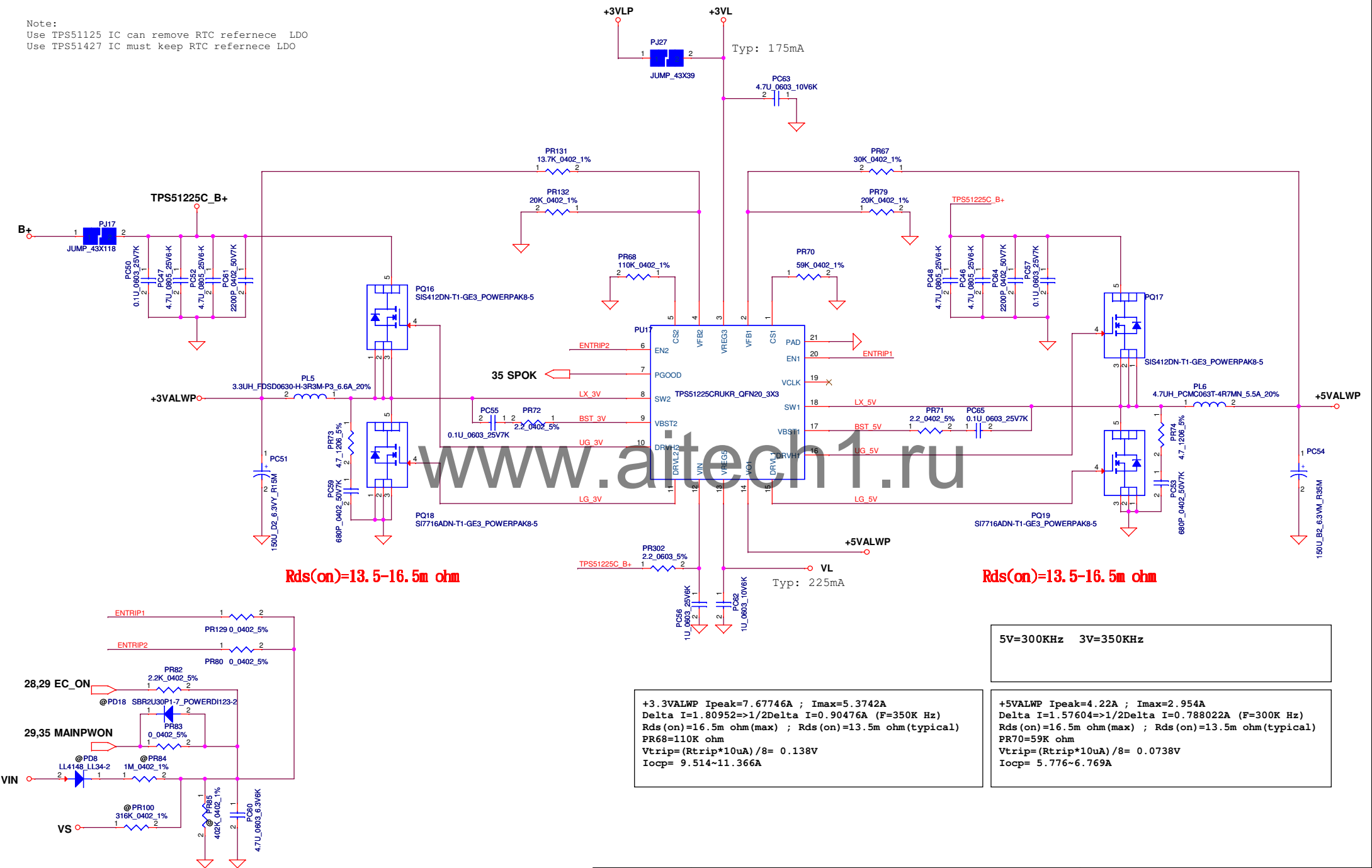


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Size		Document Number		Rev	
Custom		Chief River VC		0.1	
Date:		Friday, August 10, 2012		Sheet 34 of 52	



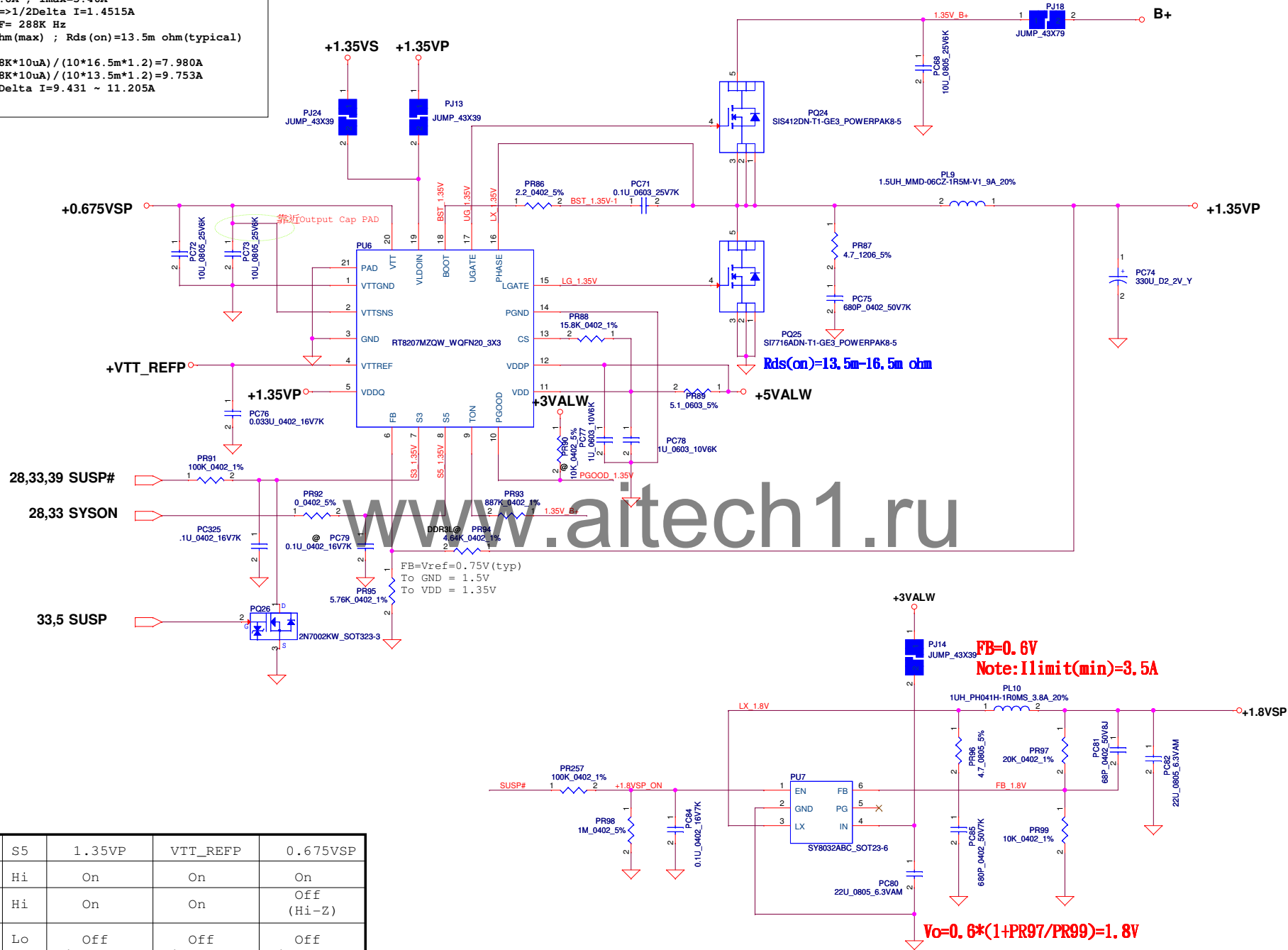
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						Size	Document Number			Rev
						Custom	Q3ZMC M/B LA-8481P Schematic			0.1
						Date:	Friday, August 10, 2012		Sheet	36

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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								Custom		Document Number		0.1	
								Date:		Friday, August 10, 2012		Sheet 37 of 52	

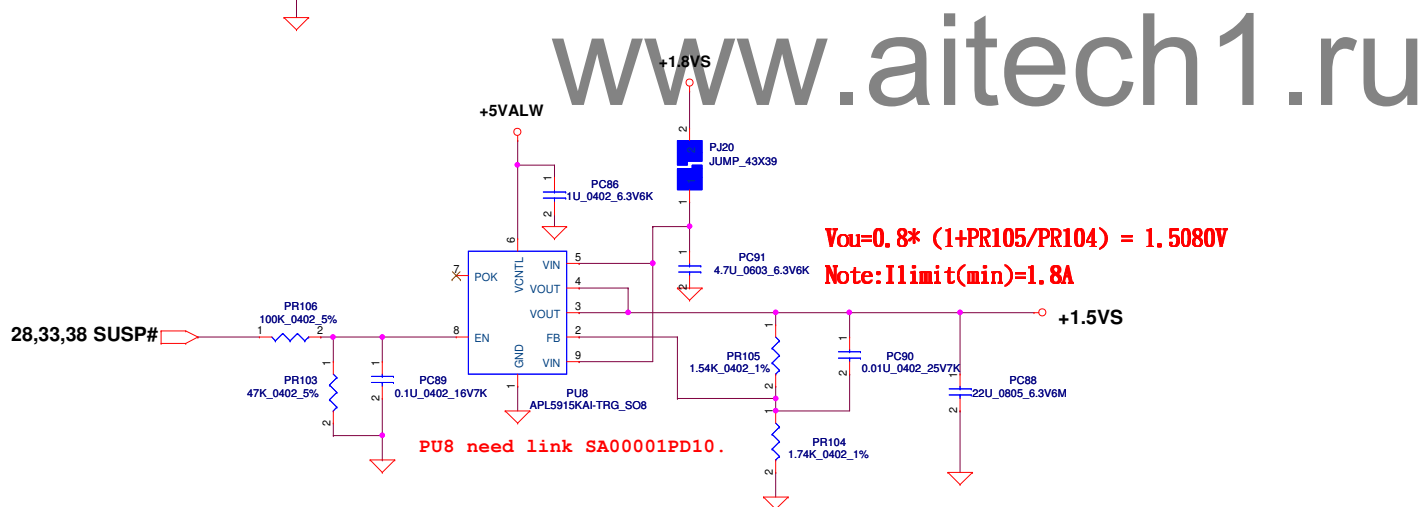
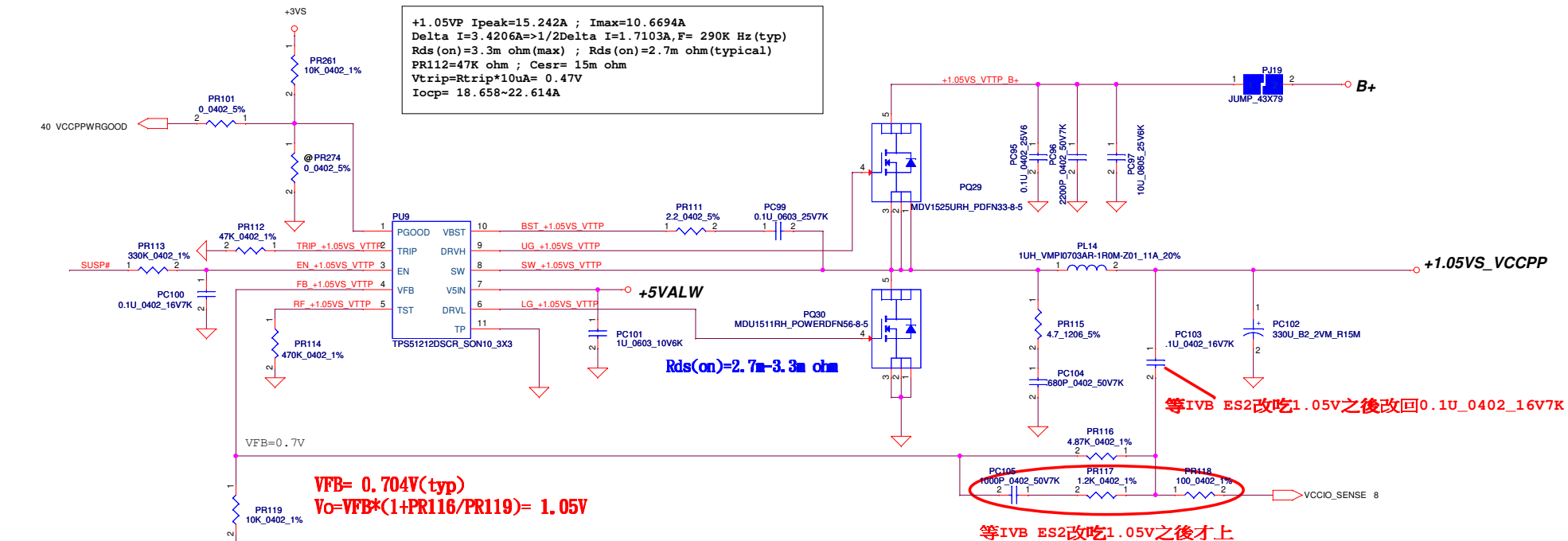
$+1.35VP$ $I_{peak}=7.8A$; $I_{max}=5.46A$
 $\Delta I=2.9030A \Rightarrow 1/2 \Delta I=1.4515A$
 $R_{ton}=887K \text{ ohm}$, $F=288K \text{ Hz}$
 $R_{ds(on)}=16.5m \text{ ohm(max)}$; $R_{ds(on)}=13.5m \text{ ohm(typical)}$
 $PR88=15.8K \text{ ohm}$
 $I_{limit_min}=(15.8K*10uA)/(10*16.5m*1.2)=7.980A$
 $I_{limit_max}=(15.8K*10uA)/(10*13.5m*1.2)=9.753A$
 $I_{ocp}=I_{limit}+1/2 \Delta I=9.431 \sim 11.205A$



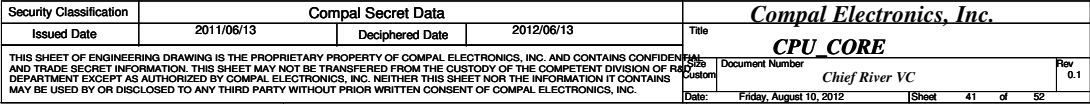
STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

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Issued Date	2011/06/13	Deciphered Date	2012/06/13	1.35VP/0.65VSP/1.8VSP	
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				Custom	0.1
				Chief River VC	
				Date:	Friday, August 10, 2012
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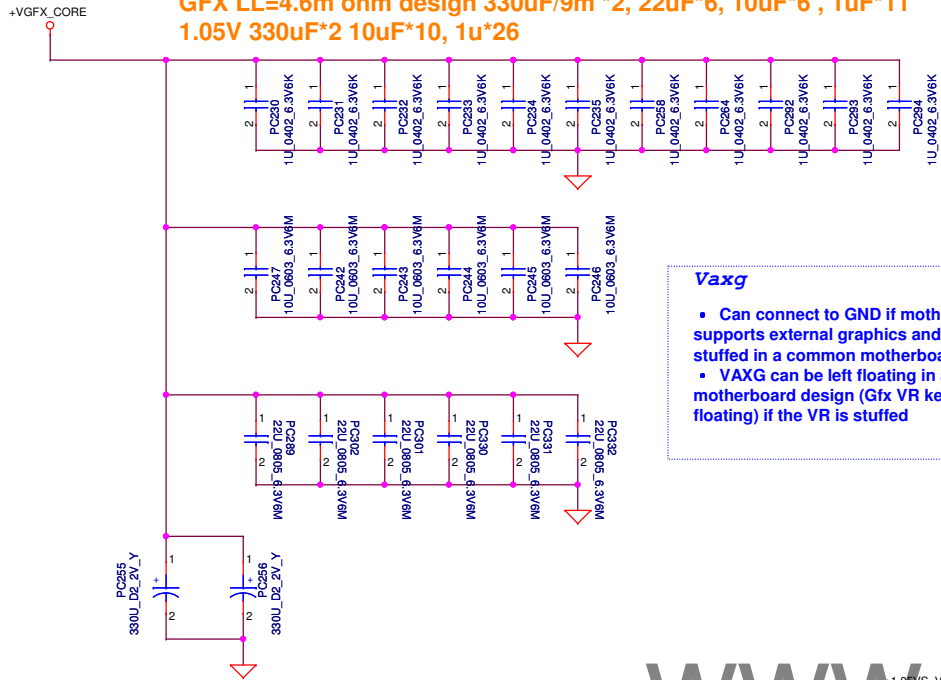


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				Document Number
				Customer
				Chief River VC
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				0.1
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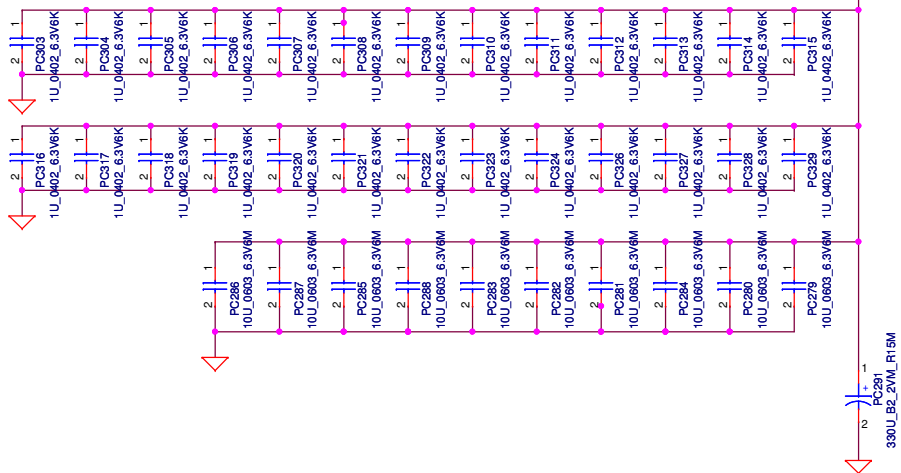
PWR Rule

CPU LL=2.9m ohm design 330uF/9m *4, 22uF *12, 2.2uF*16
GFX LL=4.6m ohm design 330uF/9m *2, 22uF*6, 10uF*6 , 1uF*11
1.05V 330uF*2 10uF*10, 1u*26



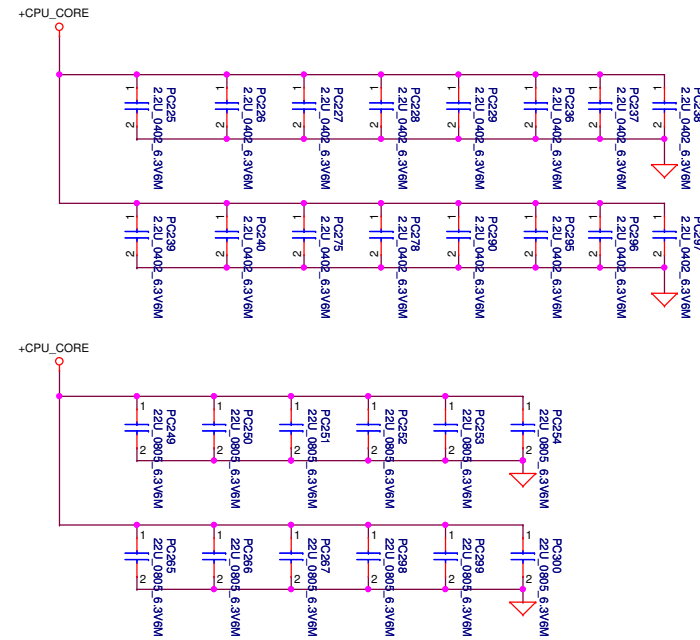
Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



INTEL Recommend

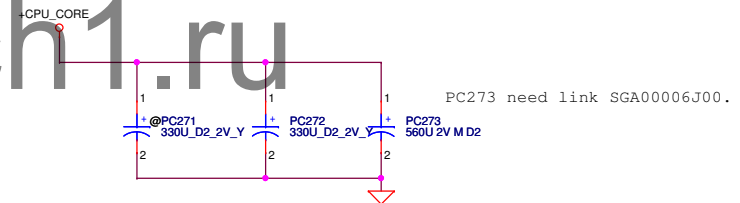
3*330uF(1 in other page),12*22uF, 5 no stuff from PDDG 1.0



For BOT side

For TOP side

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				Chief River VC	
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change Component Part Number.	Factory lack of material	0.1	41	Change PC51 to SGA00002B00(S POLY C 330U 6.3V M D2E ESR25M TPE H1.8) Change PC56 to SE000006900(S CER CAP 1UF 25V K X5R 0603)	2012/03/07	EVT
2	Add Diode	HW request add a Diode(PD18) to protection EC.	0.1	41	Add PD18 to SC100005R00(S DIO SBR2U30P1-7 POWERDI123-2)	2012/03/07	EVT
3	Adjust 3ValwP/5ValwP enable timing.	Adjust 3ValwP/5ValwP enable timing	0.1	41	Change PR83,PR84,PR85,PD8 to @PR83,@PR84,@PR85,@PD8	2012/03/07	EVT
4	Add resister and capacitor.	Adjust dynamic VID.	0.1	45	Add PR303 to SD034200180(S RES 1/16W 2K +-1% 0402) Add PC366 to SE074471K80(S CER CAP 470P 50V K X7R 0402)	2012/03/07	EVT
5	Change Function Solution.	Factory lack of material	0.1	41	Change @PR83,PD18 to PR83,@PD18	2012/03/19	EVT
6	Change CPU_Core Capacitor Solution.	Acer request reduce TOP layer highly.	0.1	41	Change PC271,@PC272 to @PC271,PC272	2012/03/19	EVT
7	Change Component Part Number.	Cost Down.	0.2	39	Change PH2&PH11 to SL200000V00(S THERM_ 100K +-1% NCP15WF104F03RC 0402)	2012/04/8	EVT2
8	Change Component Part Number.	The Component Rated Voltage Is Not Enough.	0.2	40	Change PQ8 to SB000009Q80(S TR 2N7002KW 1N SOT323-3)	2012/04/8	EVT2
9	Change Component Part Number.	Cost Down.	0.2	48	Change PC262 to SE000000F80(S CER CAP 4.7U 25V K X6S 0805 H1.25) Change PQ50 to SB000000Q00(S TR 1BS84LTI0 1P SOT23-3) Change PR181 to SD034100480(S RES 1/16W 1M +-1% 0402) Change PC263 to SE068101K80(S CER CAP 100P 25V K NPO 0402) Change PR175 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR191 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR197 to SD034100380(S RES 1/16W 100K +-1% 0402) Change PC257 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR186 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR182 to SD034100380(S RES 1/16W 100K +-1% 0402) Change PC276 to SE068102J80(S CER CAP 1000P 25V J NPO 0402)	2012/04/8	EVT2
10	Adjust LED Driver IC Sequence.	Modify LED Driver IC Sequence Error.	0.2	48	Delete PR185 & PC270. Change VIN From +5VS to B+.	2012/04/8	EVT2
11	Adjust LED Driver IC OVP.	Adjust LED Driver IC OVP Value.	0.2	48	Change PR193 to SD00000H880(S RES 1/16W 54.9K +-1% 0402)	2012/04/8	EVT2
15	Add Jumper.	For EVT2 Testing	0.2	48	Add @PJ26.	2012/04/8	EVT2
16	Adjust Boost Resistor	EMC request adjust 3VALW And 5VALW boost resistor.	0.2	41	Change PR71 to SD028220B80(S RES 1/16W 2.2 +-5% 0402) Change PR72 to SD028220B80(S RES 1/16W 2.2 +-5% 0402)	2012/04/18	EVT2
17	Adjust Snubber Function.	EMC request adjust GFX snubber function.	0.2	45	Change @PC190,@PR200 to PC190,PR200	2012/04/18	EVT2
18	Adjust Snubber Function.	EMC request adjust CPU snubber function.	0.2	45	Change @PC188,@PR195 to PC188,PR195	2012/04/18	EVT2

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Size	Document Number	Rev		0.1	
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
19	Change Component Part Number.	Cost Down.	0.2	41	Change PC51 to SGA00003700(S POLY C 150U 6.3V Y D2 LESR15M CX H1.9)	2012/04/23	EVT2
20	Add DC in Cable Part Number..	Add DC in Cable.	0.2		Add DC In Cable to DC30100L000.	2012/04/27	EVT2
21	Change Component Part Number.	Factory lack of material.	0.2	48	Change PC262 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	2012/04/27	EVT2
22	Adjust Function Voltage Output.	Project request adjustable function voltage output from 1.35V to 1.5V.	0.2	42	Change PR94 to DDR3L@ PR94.	2012/04/27	EVT2
23	Adjust Function State.	Project request selectable function state.	0.2	44	Change PC92 to TB@ PC92. Change PC93 to TB@ PC93. Change PC94 to TB@ PC94. Change PC108 to TB@ PC108. Change PC111 to TB@ PC111. Change PU16 to TB@ PU16. Change PL8 to TB@ PL8. Change PR107 to TB@ PR107. Change PR108 to TB@ PR108. Change PR109 to TB@ PR109. Change PR110 to TB@ PR110. Change PR123 to TB@ PR123. Change PR258 to TB@ PR258. Change PU11 to TB@ PU11.	2012/04/27	EVT2
24	Adjust Function State.	Project request selectable function state.	0.2	47	Change PC358 to TB@ PC358. Change PC359 to TB@ PC359. Change PC360 to TB@ PC360. Change PC361 to TB@ PC361. Change PC362 to TB@ PC362. Change PC363 to TB@ PC363. Change PC364 to TB@ PC364. Change PC365 to TB@ PC365. Change PD15 to TB@ PD15. Change PU22 to TB@ PU22. Change FL27 to TB@ FL27. Change PQ47 to TB@ PQ47. Change PQ48 to TB@ PQ48. Change PR288 to TB@ PR288. Change PR289 to TB@ PR289. Change PR290 to TB@ PR290. Change PR291 to TB@ PR291. Change PR292 to TB@ PR292. Change PR293 to TB@ PR293. Change PR294 to TB@ PR294. Change PR295 to TB@ PR295. Change PU16 to TB@ PU16.	2012/04/27	EVT2
25	Change Component Part Number.	Modify PMOS Chose Error.	0.3	48	Change PQ50 to SB000001I100(S TR P5103EMG 1P SOT23-3)	2012/05/14	DVT
26	Change Pull High Voltage.	EC request change pull high voltage from +3VALW to +3VLP.	0.3	39	Change BAIT_TEMP pull high voltage to +3VLP	2012/05/14	DVT
27	Adjust +1.35VP Soft Start Timing.	HW request adjust +1.35VP soft start timing.	0.3	42	Change PR91 to SD034100380(S RES 1/16W 100K +-1% 0402)	2012/05/16	DVT
28	Adjust CPU and VGFX Core Load Line.	Adjust CPU Core and VGFX Core Load Line.	0.3	45	Change @PC142 to PC142,SE074222K80(S CER CAP 2200P 50V K X7R 0402) Change @PC143 to PC143,SE074222K80(S CER CAP 2200P 50V K X7R 0402) Change @PR139 to PR139,SD0000008080(S RES 1/16W 649 +-1% 0402) Change @PR146 to PR146,SD0000008080(S RES 1/16W 649 +-1% 0402) Change PR187 to SD034619080(S RES 1/16W 619 +-1% 0402) Change PR135 to SD000000DN00(S RES 1/16W 330 +-1% 0402) Change PR137 to SD0000003380(S RES 1/16W 1.62K +-1% 0402)	2012/05/16	DVT

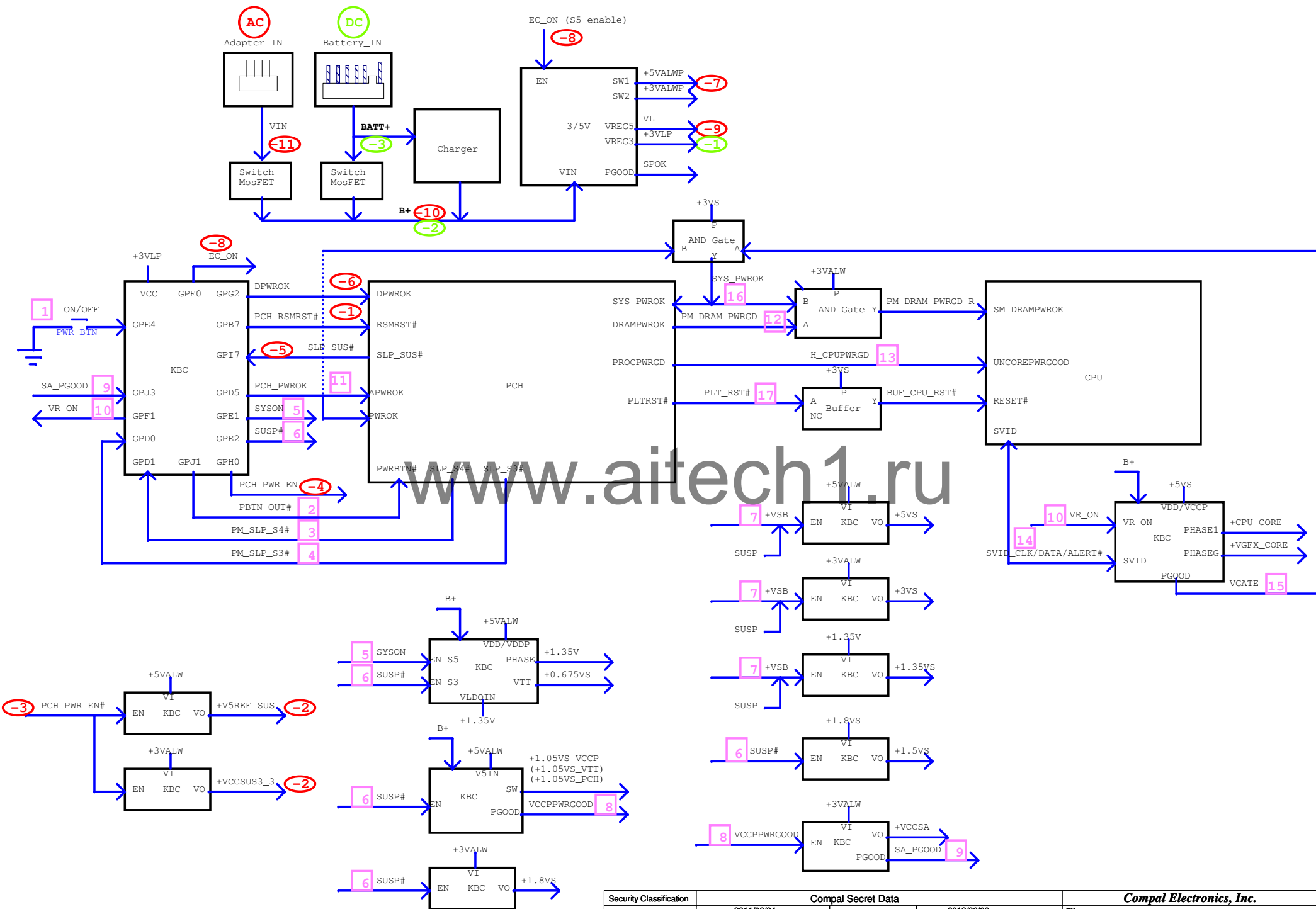
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Version change list (P.I.R. List)

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for PWR

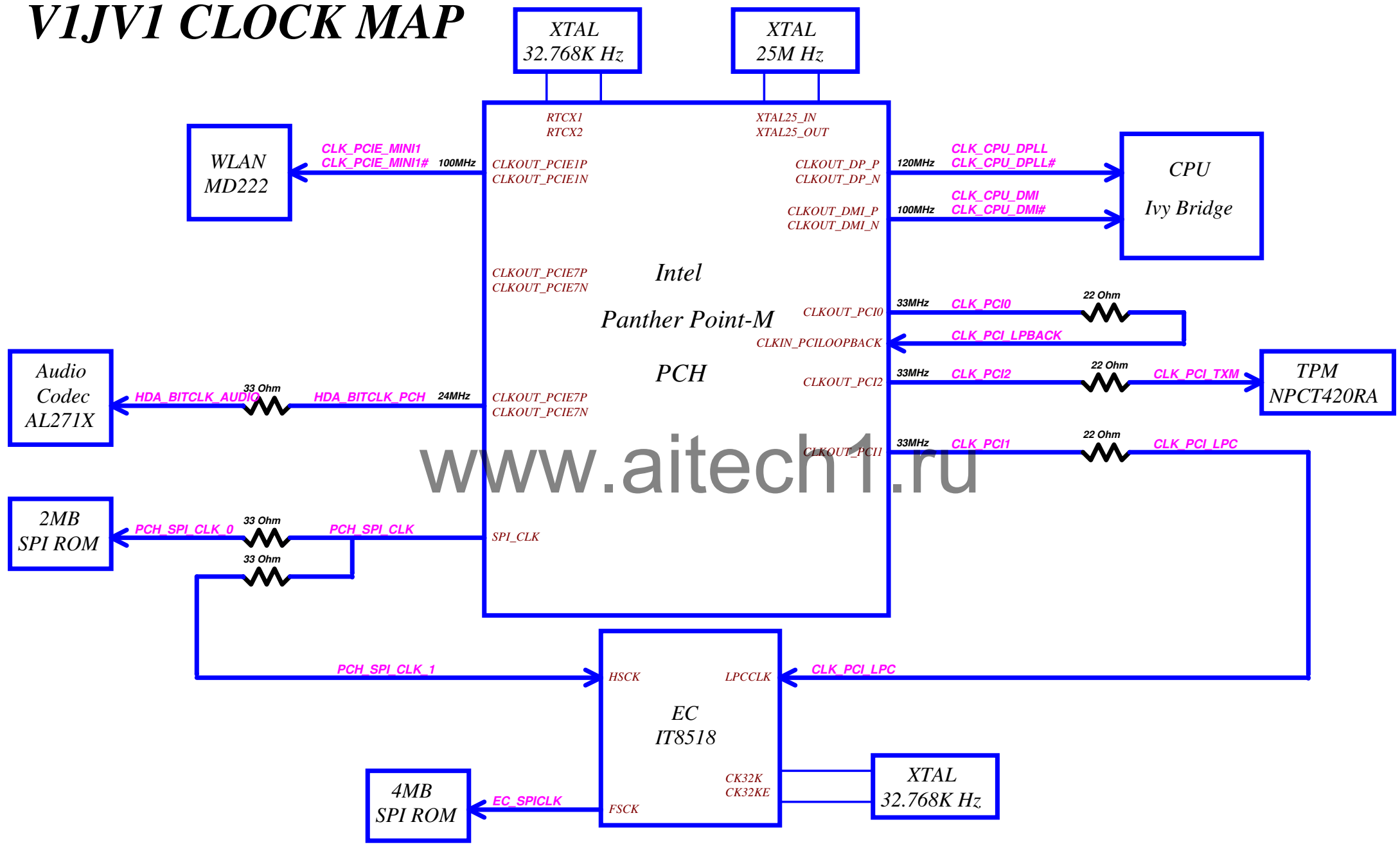
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
29	Adjust Snubber Function.	RF request adjust 3VALW And 5VALW snubber function.	0.3	41	Change @PC59,@PR73 to PC59,PR73 Change @PC53,@PR74 to PC53,PR74	2012/05/27	DVT
30	Adjust Snubber Function.	RF request adjust 1.35VP snubber function.	0.3	42	Change @PC75,@PR87 to PC75,PR87	2012/05/27	DVT
31	Adjust Snubber Function.	RF request adjust 1.05VS_VCCPP snubber function.	0.3	43	Change @PC104,@PR115 to PC104,PR115	2012/05/27	DVT
32	Adjust Snubber Function.	RF request adjust VCCSAP snubber function.	0.3	44	Change @PC109,@PR126 to PC109,PR126	2012/05/27	DVT
33	Add a resister from FB Pin to GND.	Component application demands.	0.4	48	Add PR205 to SD028000080(S RES 1/16W 0 +-5% 0402) Add PR202 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/06/17	PVT
34	Change Component Part Number.	Component application demands.	0.4	48	Change PR276 to SD034402380(S RES 1/16W 402K +-1% 0402)	2012/06/17	PVT
35	Adjust ADP_I Function Voltage Level.	Change adapter from 65W to 45W.	0.4	39	Change PR144 to SD034330280(S RES 1/16W 33K +-1% 0402) Change PR297 to SD034390280(S RES 1/16W 39K +1% 0402)	2012/06/22	PVT
36	Delete +HV_12VP Function .	Project Canceled Thunderbolt spec.	0.4	47	Delete TB@ PC358.TB@ PC359.TB@ PC360. TB@ PC361.TB@ PC362.TB@ PC363.TB@ PC364. TB@ PC365.TB@ PD15.TB@ PJ22.TB@ PL27. TB@ PQ47. TB@ PQ48.TB@ PR288.TB@ PR289. TB@ PR290.TB@ PR291.TB@ PR292.TB@ PR293. TB@ PR294.TB@ PR295.TB@ PU16.PU12	2012/06/28	PVT
37	Delete 1.05VS_LCP Function .	Project Canceled Thunderbolt spec.	0.4	40	Delete TB@ PC32.TB@ PC93.TB@ PC94.TB@ PC108. TB@ PC111.TB@ PU16.TB@ PL@ TB@ PR101. TB@ PR108.TB@ PR109.TB@ PR110.TB@ PR123. TB@ PR258.TB@ PU11.PU15	2012/06/28	PVT
38	Add a resister from ILIM Pin to +3VLP.	Component application demands.	0.4	36	Add PR59 to SD034316380(S RES 1/16W 316K +-1% 0402)	2012/07/04	PVT
39	Change Charger IC ILIM Pin of Voltage Source.	Change Charger IC ILIM Pin Voltage to +3VLP.	0.4	36	Change PR58 to @PR58.	2012/07/04	PVT
40	Add a resister from PU14 Pin3 to U53 Pin35.	Detect OTP Function For EC.	0.4	35	Add PR207 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/07/09	PVT
41	Add resister.	HW request add resister for test. (reduce DC Mode S5 power consumption)	0.4	35	Change PR208 to SD028000080(S RES 1/16W 0 +-5% 0402) Change @PR209 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR210 to SD028000080(S RES 1/16W 0 +-5% 0402) Change @PR211 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/07/09	PVT
42	Add Jump and Voltage Source Net Name.	HW request add Jump for test. (reduce DC Mode S5 power consumption)	0.4	37	Add PJ27 from +3VL to +3VLP.	2012/07/10	PVT
43	Change Component Part Number.	Factory lack of material	0.4	39	Change PU8 to SA00001PD10(S IC APL5915KAI-TRG SO 8P)	2012/07/17	PVT
44	Change Component Part Number.	Factory lack of material	0.5	43	Change PC277 to SE071101J80(S CER CAP 100P 50V J NPO 0402) Change PC263 to SE071101J80(S CER CAP 100P 50V J NPO 0402)	2012/07/30	PVT2

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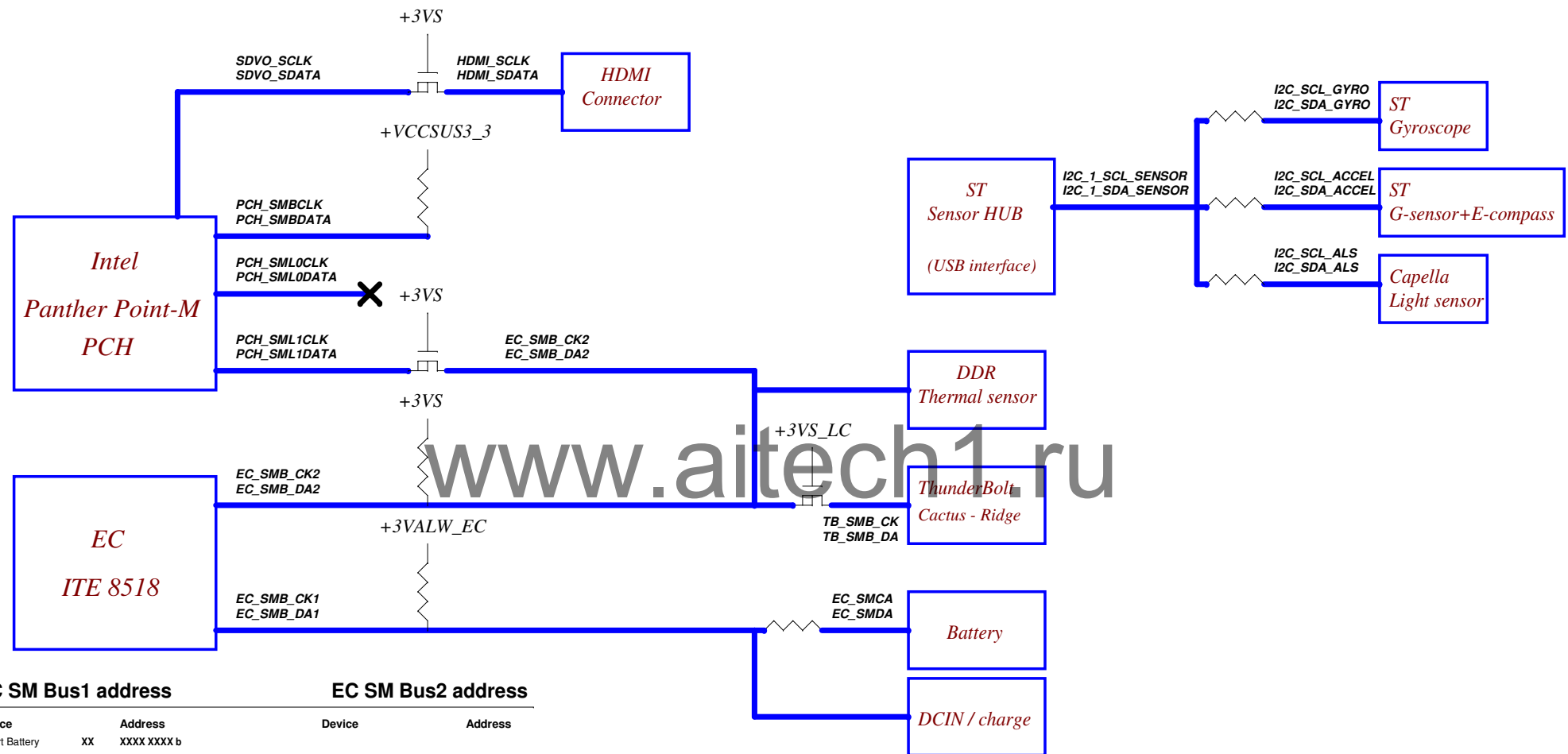


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V1JV1 CLOCK MAP



SMBUS Block Diagram



EC SM Bus1 address

Device	Address
Smart Battery	XX XXXX XXXX b
DCIN / Charge	13 0001 001X b

EC SM Bus2 address

Device	Address
DDR Thermal sensor	99 1001 101X b
Thunderbolt	29 0010 100X b(CIO P1)
	2B 0010 101X b(CIO P2)
	2D 0010 110X b(CIO P3)
	2F 0010 111X b(CIO P4)

PCH SM Bus address

Device	Address
ST sensor HUB	XX XXXX XXXX b

PCH SM Bus address(Link 1)

Device	Address
DDR Thermal sensor	99 1001 101X b
Thunderbolt	29 0010 100X b(CIO P1)
	2B 0010 101X b(CIO P2)
	2D 0010 110X b(CIO P3)
	2F 0010 111X b(CIO P4)

Sensor HUB SM Bus address

Device	Address
Gyroscope	D1 1101 000X b
	D3 1101 001X b
E-compass + G sensor	33 0011 001X b
ALS sensor	21 0010 000X b

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
EVT2					DVT-continue	Pre MP	
01. Change component Part Number base on EVT SMT Memo					12. Add 18pF-0201 capacitors (5pcs) to PCH power rail (RF requirement)	01. Change SW2 to SN200003200/SSS12-LGF-Q-T-R as ME request (Silder SW)	
a. Change D22,D23 form SC500004B00 to SC500005I00					13.Change below part BOM structure base on power sequence requirement	02. Add Clip at DDR_Ch_B(avoid DDR solder crack)	
b. Change Q20 from SB000009Q80 to SB000002X00					a. Unstuff R81 / stuff R82 (SM_DRAMPWROK)	03. Add series resistor & capacitor to PLT_RST# at PCH side	
02. Modify JHDB1.8 pin to HUB_RST#					b. Unstuff R487 / stuff R493 (APWROK)	04. Stuff C1209, C764 (PLT_RST#)	
03. Reserve 0_0603 resistor(R572 / R562, un-stuff) to GND for ME/CMOS clear at TOP side					14. Change Q76 to AP2301 (SB000007H10) / R837 change to 100K	05. Remove R371, R464 that un-used	
04. C744,C745,C1338,C1340 PCB Footprint modify as C_0402NEW					15. Change R287/R299 to 1K (Debug port)	06. Change R14 to 150 ohm, R8 to 1.5k ohm base on LED brightness test	
05. Reserve 0 ohm resistor to JED1.26(R465, un-stuff), touch screen control board request					16. Change R960 to 18K (Board ID update)	07. Update BOM option base on PVT SMT memo	
06. Reserve SA_PG00D connection to APWROK for sequence testing					17. Unstuff un-used components -SW3 / SW5	a. Stuff R427, un-stuff R943 for WLAN wake# power rail	
07. Change R299, R287 to 2K ohm(for Debug function)					18. Change H7 to H_3P0N	b. Un-stuff R459(HUB_RST#) base on Intel Sensor DG 0.85	
08. Reserve JEC1 connector for SW debug					19. Unstuff C1463, C1469, C1495, C1493, C1500, C1486, C1475, C1485, C990, C970, C472, C460, C375,	c. Un-stuff R524, stuff R240 (Gyro_SA0) base on Intel Sensor suggestion	
09. Update JUSB1, JTB1, JHDMI1 connector for ME requirement					20. Unstuff R1137, Change R1056 to 100k base on Acer requirement	d. Change R481(Accel_Int) PD resistor to 100k base on Intel Sensor DG 0.85	
10. Thunderbolt Led related circuit change connection from PCH to EC					21. Change R1083, R1078, R1089, R1080, R1081, R1082, R1086, L66 to 0 Ohm resistors (Base on TBT CRB Rev1.24)	08. Add series resistor to PLT_RST# at EC side	
11. Add pull up resistor to IRST_RST# at EC side					22. CHANGE C394/C1000 from SGA00001E00 to SGA00002N80	09. JHDMI1 BOM structure as CONN@	
12. Reserve VR_ON connection to U5.2 for sequence testing					23. Unstuff C5, C8, R18, R86 (eDP BKOFF#/INVT PWM#)	10. Update PCB PN as DAZ0SM00100 / PCB V1JV1 LA-9011P LS-9011P	
13. Add soft-start for PCH VCCSU53_3, V5REF_SUS power rail enable					24. Stuff R706, R707, unstuff L68 (Sensor fusion USB interface)	11. Change R960 to 100k (Board ID update)	
14. Reserve tact switch at developing pahse(MP remove)					25. Update DDR ID Table (X76@) / CH-B DRAMS BOM structure change to 128@	12. Unstuff Touch screen power switch circuit (not used)	
15. Change R960 to 8.2k (board ID update for EVT2)					26. Update TBT schematic (Security Level control by PCH)	13. Unstuff external wireless KB power switch circuit (not used)	
16. Stuff R699, R700 for EC debug					/ unstuff un-used components - R1036/R1037/R406/R657	14. Change 0 ohm resistors as short-pad (0805x2 , 0603x5, 0402x73)	
17. R1130, R1131, R1132 change to TB@					27. Change LED PN(Lite-On / SC50000CF00)	0805 -> R477,R968	
18. Reserve TB GPIO pin connection to PCH/EC colay						0603 -> R969,R970,R971,R972,R982	
19. U65 (TB-32k ROM) part description/value correct						0402 -> R3,R80,R241,R249,R256,R258,R270,R276,R280,R314	
20. Up components size shown as below						R320,R394,R418,R462,R463,R488,R491,R492,R494,R496	
Capacitors from 0201 to 0402 : (Total 59)						R498,R501,R504,R565,R571,R575,R577,R578,R579,R581	
C507, C503, C506, C504, C445, C444, C488, C489, C1510, C1487						R582,R584,R585,R586,R591,R593,R612,R622,R626,R627	
C1301, C1471, C1476, C1295, C1488, C1294, C1299, C1489, C1298, C1253,						R630,R631,R661,R692,R696,R697,R698,R705,R706,R707	
C1254, C1252, C583, C584, C376, C377, C338, C102, C1373, C462,						R710,R713,R724,R725,R726,R753,R785,R792,R795,R796	
C447, C487, C481, C630, C483, C448, C446, C1218, C587, C579,						R797,R798,R799,R940,R951,R977,R979,R983,R984,R987	
C1508, C1297, C1498, C1497, C1477, C1478, C1492, C1491, C1470, C1468,						R1323,R1324,R1327,	
C647, C8, C539, C1198, C1200, C442, C324, C441, C1499							
Resistors form 0201 to 0402 : (Total 11)						15. Base on Intel Sensor DG1.0 , modify below item	
R467, R488, R492, R494, R1113, R712, R711, R1115, R1116, R1079,						a. Add series resistor between HUB_DBG_PB4 / HUB_RST#	
R1023						b. R453, R466 tolerance as 1%	
						c. C462,R1329,C402,C508,C481,C483,C485,C487,C503,C504,C506,C507 tolerance as 10%	
21. Change Q3 form SB039040000 to SB000006A00 (SB039040000 EOL)						16. Change U140 to SA00005P210 / S IC STM32F103RCY6TRC16 WLCSP MCU V1JV1 (ST sensor Hub with Intel F/W for V1JV1 use only)	
22. Change R717,R718 to 60.4 ohm (base on audio test)						17. Define GPIO69/70 to TPM table	
23. Change component Part Number base on EVT2 SMT Memo							
a. Change D6 from SC1H751H010 to SC500000Z00							
b. Change R2 from SD028100180 to SD028100280							
c. Change C6 from SE076473K80 to SE000000K80							
d. Change R5 from SD013300080 to SD013150080							
24. R495 change to 0 ohm resistor, C1464 un-stuff							
25. Update PN of CPU/TB-Catcus Ridge for EVT2							
DVT					PVT		
01. Reserve connection between PCH SUS_STAT# & TPM/TCM LPCPD#					01. Unstuff R1318 base on Intel suggestion. (Sensor Hub Reset#)		
02. Change JFAN1 to SP02000H700 / S W-CONN ACES 88231-04001 4P P1.25					02. Add Lite-On MD222 PN for BOM optional		
03. Base on EMI request, change below ESD PN					03. Change U142 BOM structure to TB@		
a. Change D55, D56, D57, D59 to SCA00001W00					04. Add +3VALW power to LED		
b. Change D3, D7, D13, D42, D43, D44, D35 to SC300002800					05. PID/BID Power domain change to +3VALW_EC		
04. Reserve HOME_KEY, VOL_UP/DOWN, D_LOCK connection to PCH					06. Remove TBT function / circuit		
05. Reserve both 5V / 3.3V to rear camera					07. Change JFAN1 from SP02000H700 to SP01001B200 (ME/Thermal request)		
06. Add series resistor to DC/DC					08. Reserve sensor hub usb_d+ connection to U140.A5 by 1.5k resistor		
07. Change WLAN PCIe port to port1					09. Correct SPI ROM part description/value (U40,U42)		
08. Change RST IC solution to GMT-G696L					10. Change R960 to 33K (Board ID update)		
09. LED circuit update					11. Change Touch Screen USB port to port3		
10. Add Schottky Rectifier to +HV_12V (TB CRB update)					12. Change eDP Connector to I-PEX_20455-030E (ME connector list)		
11. Remove C377, C376					13. Reserve Touch Screen power +5V_TS for touch wake support		
					14. Change SW1/SW4/SW4 to SN100006Y00		
					15. Change JSPK1,JFAN1 to SP01000Q810 as ME connector list		
					16. Reserve JEC2 connector for EC debug		
					17. Reserve JEXT1 connector for BT/KB function		
					18. Reserve EC Reset function		
					19. Update sensor fusion base on Intel DG R0.85		
					20. Change R269 from 200k to 33k and R636 from 0 ohm to 10k for S3 resume sequenece fine tune		
					21. For D55 power consumption reduce, change below resistor to 100k ohm		
					R939 (EC_SMI# PU) / R667 (DPWROK PD) / R341 (PCH_ACIN)		
					R259 (PWR_LED# / R260 (BATT_AMB_LED# NMOS pull H) / R506 (PCH_GPIO27)		
					R955 (BVOL_UP#_R PU) / R956 (VOL_DOWN#_R PU) / R959 (HOME_KEY PU)		
					22. Unstuff R699/R700 (EC debug connector series resistor)		
					23. Unstuff D18 (unused component)		
					24. Add UCPU1 PN for PVT (I3-2365)		
					25. Change PCH PN from SA00005AG00 (QS) to SA00005AG10 (R3)		

Pre MP

PCB

ZZZ1 LA-9011P MB Rev0: DAA00004F00
LA-9011P MB Rev1: DAA00004F10
LA-9011P MB with Small Board Rev1: DAZ0SM00100
LA-9011P LS-9011P REV1
DAZ0SM00100

WLAN/BT Module

U1 LIONMD222@
PK29S004B10
S_W/L_MOD WCBN3501A W/BT MD222 ABO!
WCBN3501A W/BT MD222

CPU

UCPU1 S IC AV8063801058001 QC55 L0 1.7G ABO! EVT
I53317@ SA00005K630
AV8063801058001 QC55 L0 1.7G ABO!

UCPU1 S IC AV8063801057800 QC54 L0 1.8G ABO! EVT
I53427@ SA00005L920
AV8063801057800 QC54 L0 1.8G ABO!

UCPU1 S IC AV8063801057604 QC53 L0 1.9G ABO! EVT
I73517@ SA00005K520
AV8063801057604 QC53 L0 1.9G ABO!

UCPU1 S IC AV8062701147601 QB31 J1 1.5G ABO! EVT2
B987@ SA00005QH10 Sandy Bridge Processor
For EVT2 SKU2
AV8062701147601 QB31 J1 1.5G ABO!

UCPU1 S IC AV8063801058002 QC9E L1 1.7G ABO!
I53317U@ SA00005K680
AV8063801058002 QC9E L1 1.7G ABO!

UCPU1 S IC AV8063801058401 SR0N9 L1 1.8G ABO! DVT PVT
I33217@ SA00005L5C0
AV8063801058401 SR0N9 L1 1.8G ABO!

UCPU1 S IC AV8063801058401 QC9F L1 1.8G ABO! DVT
I33217Q@ SA00005L580
AV8063801058401 QC9F L1 1.8G ABO!

UCPU1 S IC AV8063801058002 SR0N8 L1 1.7G ABO! DVT PVT
I53317S@ SA00005K6B0
AV8063801058002 SR0N8 L1 1.7G ABO!

UCPU1 S IC AV8062701047904 SR0CV J1 1.4G ABO! PVT
I32365@ SA000051H60
AV8062701047904 SR0CV J1 1.4G ABO!

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				Custom	V1JV1 M/B LA-9011P Schematic	0.1
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